

DM74LS194A 4-Bit Bidirectional Universal Shift Register

General Description

This bidirectional shift register is designed to incorporate virtually all of the features a system designer may want in a shift register; they feature parallel inputs, parallel outputs, right-shift and left-shift serial inputs, operating-mode-control inputs, and a direct overriding clear line. The register has four distinct modes of operation, namely:

- Parallel (broadside) load
- Shift right (in the direction Q_A toward Q_D)
- Shift left (in the direction Q_D toward Q_A)
- Inhibit clock (do nothing)

Synchronous parallel loading is accomplished by applying the four bits of data and taking both mode control inputs, S_0 and S_1 , HIGH. The data is loaded into the associated flip-flops and appear at the outputs after the positive transition of the clock input. During loading, serial data flow is inhibited.

Shift right is accomplished synchronously with the rising edge of the clock pulse when S_0 is HIGH and S_1 is LOW. Serial data for this mode is entered at the shift-right data input. When S_0 is LOW and S_1 is HIGH, data shifts left synchronously and new data is entered at the shift-left serial input.

Clocking of the flip-flop is inhibited when both mode control inputs are LOW.

Features

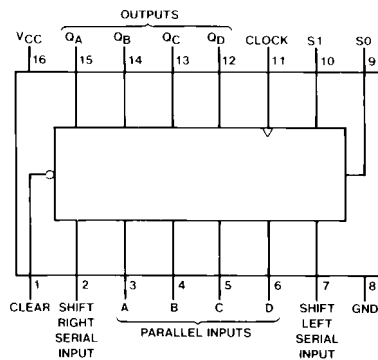
- Parallel inputs and outputs
- Four operating modes:
 - Synchronous parallel load
 - Right shift
 - Left shift
 - Do nothing
- Positive edge-triggered clocking
- Direct overriding clear

Ordering Code:

| Order Number | Package Number | Package Description |
|--------------|----------------|---|
| DM74LS194AM | M16A | 16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150 Narrow |
| DM74LS194AN | N16E | 16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide |

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Connection Diagram

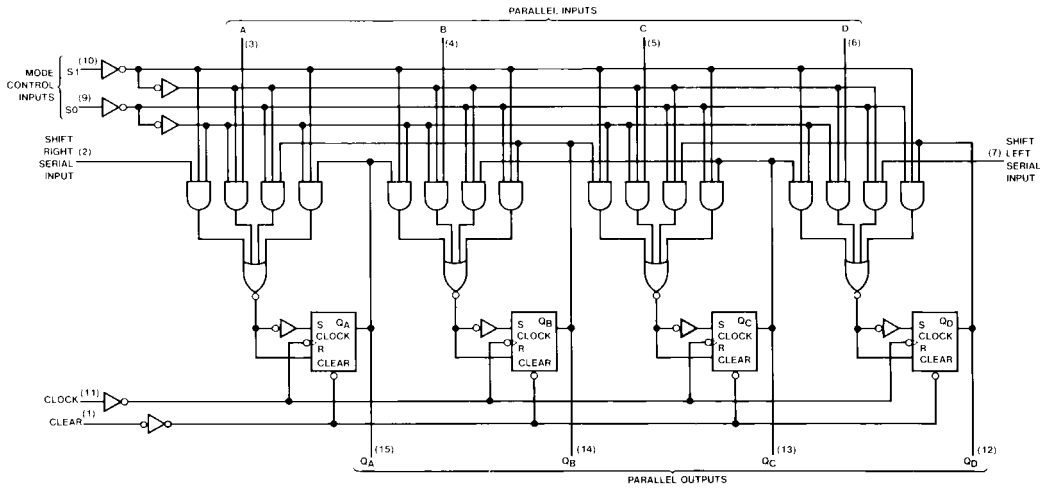


Function Table

| Clear | Mode | | Clock | Inputs | | | | Outputs | | | | | |
|-------|------|-------|-------|--------|---|----------|---|----------------|----------------|-----------------|-----------------|-----------------|-----------------|
| | | | | Serial | | Parallel | | Q _A | Q _B | Q _C | Q _D | | |
| | Left | Right | | A | B | C | D | | | | | | |
| L | X | X | X | X | X | X | X | X | X | L | L | L | L |
| H | X | X | L | X | X | X | X | X | X | Q _{A0} | Q _{B0} | Q _{C0} | Q _{D0} |
| H | H | H | ↑ | X | X | a | b | c | d | a | b | c | d |
| H | L | H | ↑ | X | H | X | X | X | X | H | Q _{An} | Q _{Bn} | Q _{Cn} |
| H | L | H | ↑ | X | L | X | X | X | X | L | Q _{An} | Q _{Bn} | Q _{Cn} |
| H | H | L | ↑ | H | X | X | X | X | X | Q _{Bn} | Q _{Cn} | Q _{Dn} | H |
| H | H | L | ↑ | L | X | X | X | X | X | Q _{Bn} | Q _{Cn} | Q _{Dn} | L |
| H | L | L | X | X | X | X | X | X | X | Q _{A0} | Q _{B0} | Q _{C0} | Q _{D0} |

H = HIGH Level (steady state)
 L = LOW Level (steady state)
 X = Don't Care (any input, including transitions)
 ↑ = Transition from LOW-to-HIGH level
 a, b, c, d = The level of steady state input at inputs A, B, C or D, respectively.
 Q_{A0}, Q_{B0}, Q_{C0}, Q_{D0} = The level of Q_A, Q_B, Q_C, or Q_D, respectively, before the indicated steady state input conditions were established.
 Q_{An}, Q_{Bn}, Q_{Cn}, Q_{Dn} = The level of Q_A, Q_B, Q_C, respectively, before the most-recent ↑ transition of the clock.

Logic Diagram



Absolute Maximum Ratings (Note 1)

| | |
|--------------------------------------|-----------------|
| Supply Voltage | 7V |
| Input Voltage | 7V |
| Operating Free Air Temperature Range | 0°C to +70°C |
| Storage Temperature Range | -65°C to +150°C |

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Recommended Operating Conditions

| Symbol | Parameter | Min | Nom | Max | Units |
|------------------|--------------------------------|-------|-----|------|-------|
| V _{CC} | Supply Voltage | 4.75 | 5 | 5.25 | V |
| V _{IH} | HIGH Level Input Voltage | 2 | | | V |
| V _{IL} | LOW Level Input Voltage | | | 0.8 | V |
| I _{OH} | HIGH Level Output Current | | | -0.4 | mA |
| I _{OL} | LOW Level Output Current | | | 8 | mA |
| f _{CLK} | Clock Frequency (Note 2) | 0 | | 25 | MHz |
| | Clock Frequency (Note 3) | 0 | | 20 | |
| t _w | Pulse Width (Note 4) | Clock | 20 | | ns |
| | | Clear | 20 | | |
| t _{SU} | Setup Time (Note 4) | Mode | 30 | | ns |
| | | Data | 20 | | |
| t _H | Hold Time (Note 4) | 0 | | | ns |
| t _{REL} | Clear Release Time (Note 4) | 25 | | | ns |
| T _A | Free Air Operating Temperature | 0 | | 70 | °C |

Note 2: C_L = 15 pF, T_A = 25°C and V_{CC} = 5V.

Note 3: C_L = 50 pF, R_L = 2 kΩ, T_A = 25°C and V_{CC} = 5V.

Note 4: T_A = 25°C and V_{CC} = 5V.

Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

| Symbol | Parameter | Conditions | Min | Typ (Note 5) | Max | Units |
|-----------------|-----------------------------------|--|-----|--------------|------|-------|
| V _I | Input Clamp Voltage | V _{CC} = Min, I _I = -18 mA | | | -1.5 | V |
| V _{OH} | HIGH Level Output Voltage | V _{CC} = Min, I _{OH} = Max | 2.7 | 3.4 | | V |
| | | V _{IL} = Max, V _{IH} = Min | | | | |
| V _{OL} | LOW Level Output Voltage | V _{CC} = Min, I _{OL} = Max | | 0.35 | 0.5 | V |
| | | V _{IL} = Max, V _{IH} = Min | | | | |
| | | I _{OL} = 4 mA, V _{CC} = Min | | | | |
| I _I | Input Current @ Max Input Voltage | V _{CC} = Max, V _I = 7V | | | 0.1 | mA |
| I _{IH} | HIGH Level Input Current | V _{CC} = Max, V _I = 2.7V | | | 20 | μA |
| I _{IL} | LOW Level Input Current | V _{CC} = Max, V _I = 0.4V | | | -0.4 | mA |
| I _{OS} | Short Circuit Output Current | V _{CC} = Max (Note 6) | -20 | | -100 | mA |
| I _{CC} | Supply Current | V _{CC} = Max (Note 7) | | 15 | 23 | mA |

Note 5: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 6: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 7: With all outputs open, inputs A through D grounded, and 4.5V applied to S0, S1, CLEAR, and the serial inputs, I_{CC} is tested with momentary ground, then 4.5V applied to CLOCK.

Switching Characteristics

at $V_{CC} = 5V$ and $T_A = 25^\circ C$

| Symbol | Parameter | From (Input) To (Output) | $C_L = 50 \text{ pF}, R_L = 2 \text{ k}\Omega$ | | Units |
|-----------|--|-----------------------------|--|-----|-------|
| | | | Min | Max | |
| f_{MAX} | Maximum Clock Frequency | | 20 | | MHz |
| t_{PLH} | Propagation Delay Time LOW-to-HIGH Level Output | Clock to Any Q | | 26 | ns |
| t_{PHL} | Propagation Delay Time HIGH-to-LOW Level Output | Clock to Any Q | | 35 | ns |
| t_{PHL} | Propagation Delay Time HIGH-to-LOW Output | Clear to Any Q | | 38 | ns |

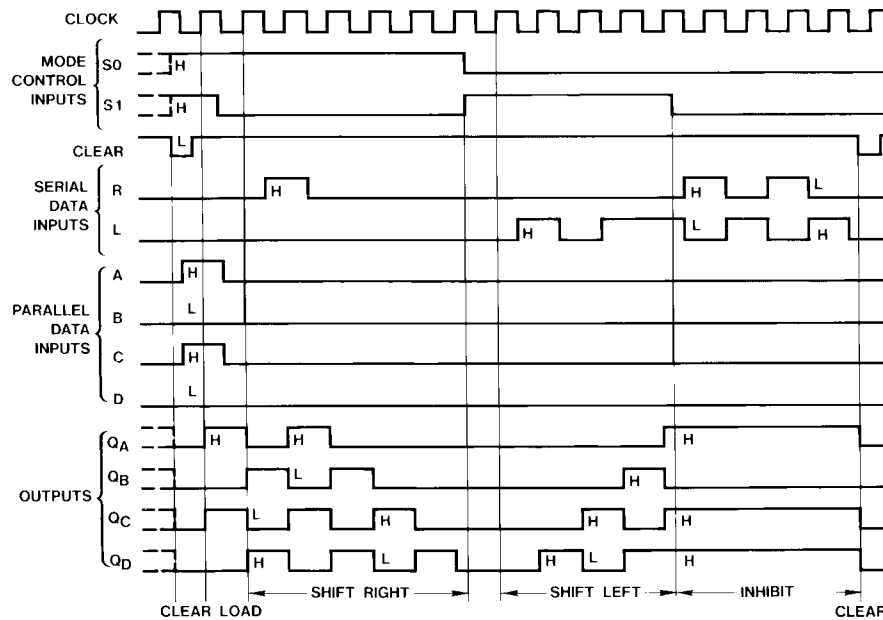
Note 8: All typicals are at $V_{CC} = 5V, T_A = 25^\circ C$.

Note 9: Not more than one output should be shorted at a time, and the duration should not exceed one second.

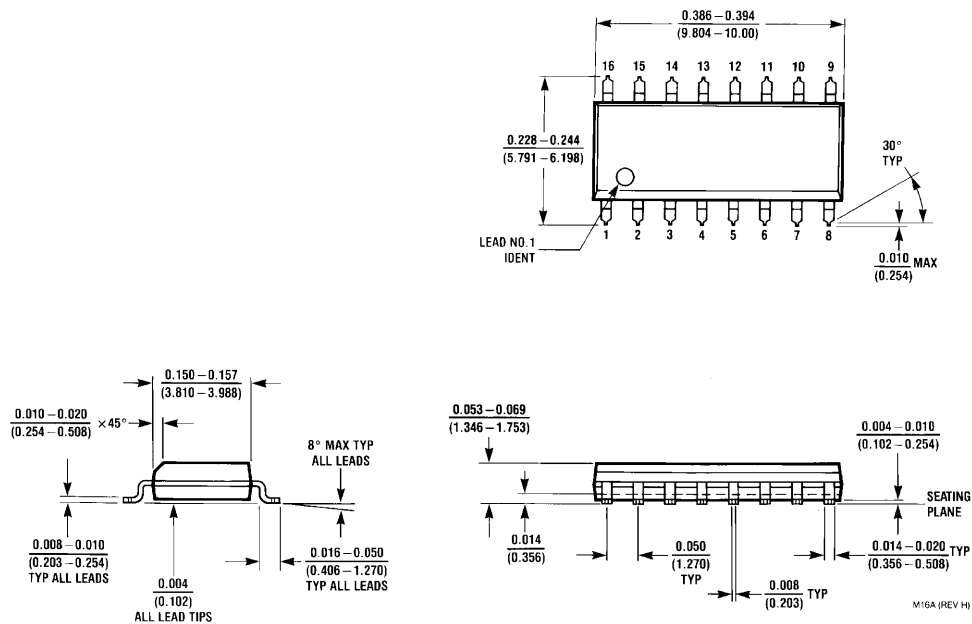
Note 10: With all outputs open, inputs A through D grounded, and 4.5V applied to S0, S1, CLEAR, and the serial inputs, I_{CC} is tested with momentary ground, then 4.5V applied to CLOCK.

Timing Diagram

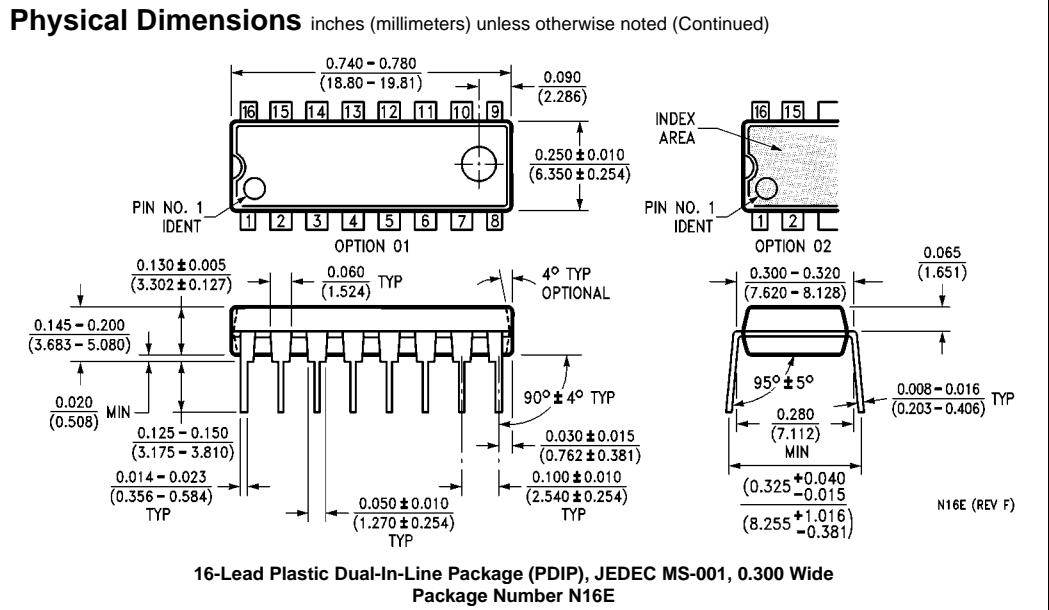
Typical Clear, Load, Right-Shift, Left-Shift, Inhibit, and Clear Sequences



Physical Dimensions inches (millimeters) unless otherwise noted



16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150 Narrow Package Number M16A



Fairchild does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied and Fairchild reserves the right at any time without notice to change said circuitry and specifications.

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

www.fairchildsemi.com

This datasheet has been downloaded from:

www.DatasheetCatalog.com

Datasheets for electronic components.