

October 1988 Revised March 2000

# **DM74LS573** Octal D-Type Latch with 3-STATE Outputs

#### **General Description**

The DM74LS573 is a high speed octal latch with buffered common Latch Enable (LE) and buffered common Output Enable (OE) inputs.

This device is functionally identical to the DM74LS373, but has different pinouts.

#### **Features**

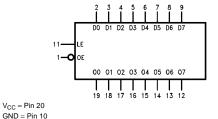
- Inputs and outputs on opposite sides of package allowing easy interface with microprocessors
- Useful as input or output port for microprocessors
- Functionally identical to DM74LS373
- Input clamp diodes limit high speed termination effects
- Fully TTL and CMOS compatible

## **Ordering Code:**

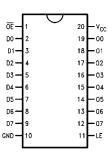
Order Number	Package Number	Package Description
DM74LS573WM	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide
DM74LS573N	N20A	20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

# **Logic Symbol**



# **Connection Diagram**



#### **Pin Descriptions**

Pin Names	Description
D0-D7	Data Inputs
	Latch Enable Input (Active HIGH)
OE	3-STATE Output Enable Input (Active LOW)
O0-O7	3-STATE Latch Outputs

#### **Function Tables**

Output Enable	Latch Enable	D	Output O
L	Н	Н	Н
L	Н	L	L
L	L	X	$Q_{O}$
Н	Х	Χ	Z

- I = I OW State
- H = HIGH State

- Z = High Impedance State
  Q<sub>O</sub> = Previous Condition of O

# **Absolute Maximum Ratings**(Note 1)

Supply Voltage 7V Input Voltage 7V Operating Free Air Temperature Range  $0^{\circ}\text{C to } +70^{\circ}\text{C}$  Storage Temperature Range  $-65^{\circ}\text{C to } +150^{\circ}\text{C}$ 

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

### **Recommended Operating Conditions**

Symbol	Parameter	Min	Nom	Max	Units
V <sub>CC</sub>	Supply Voltage	4.75	5	5.25	V
V <sub>IH</sub>	HIGH Level Input Voltage	2			V
V <sub>IL</sub>	LOW Level Input Voltage			0.8	V
I <sub>ОН</sub>	HIGH Level Input Current			-2.6	mA
I <sub>OL</sub>	LOW Level Output Current			24	mA
T <sub>A</sub>	Free Air Operating Temperature	0		70	°C

#### **Electrical Characteristics**

Over recommended operating free air temperature range (unless otherwise noted)

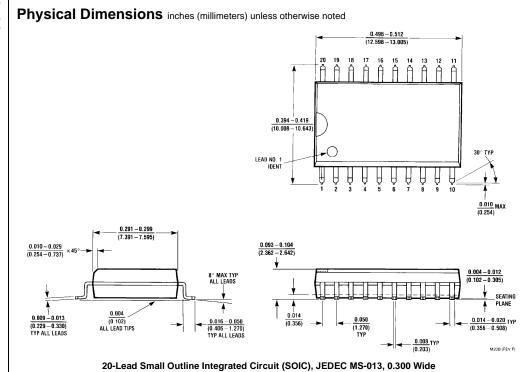
Symbol	Parameter	Conditions	Min	Typ (Note 2)	Max	Units
VI	Input Clamp Voltage	$V_{CC} = Min, I_I = -18 \text{ mA}$			-1.5	V
V <sub>OH</sub>	HIGH Level	V <sub>CC</sub> = Min, I <sub>OH</sub> = Max,	2.7	2.4		V
	Output Voltage	V <sub>IL</sub> = Max	2.1			v v
V <sub>OL</sub>	LOW Level	V <sub>CC</sub> = Min, I <sub>OL</sub> = Max,		0.25	0.5	V
	Output Voltage	$V_{IH} = Min$		0.35		
		I <sub>OL</sub> = 4 mA, V <sub>CC</sub> = Min		0.25	0.4	
I	Input Current @ Max Input Voltage	$V_{CC} = Max, V_I = 7V$			1	mA
I <sub>IH</sub>	HIGH Level Input Current	$V_{CC} = Max, V_I = 2.7V$			20	μΑ
I <sub>IL</sub>	LOW Level Input Current	$V_{CC} = Max, V_I = 0.4V$			-0.4	mA
los	Short Circuit	V <sub>CC</sub> = Max	-30		-130	mA
	Output Current	(Note 3)	-30			
Icc	Supply Current	V <sub>CC</sub> = Max			50	mA
l <sub>OZH</sub>	3-STATE Output	V <sub>CC</sub> = V <sub>CCH</sub>		1 00	20	μА
	OFF Current HIGH	$V_{OZH} = 2.7V$			20	
l <sub>OZL</sub>	3-STATE Output	$V_{CC} = V_{CCH}$			-20	μА
	OFF Current LOW	$V_{OZL} = 0.4V$				

Note 2: All typicals are at  $V_{CC} = 5V$ ,  $T_A = 25$ °C.

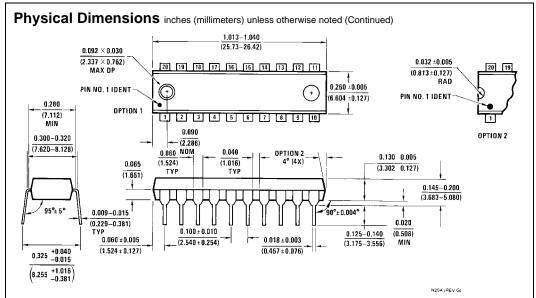
Note 3: Not more than one output should be shorted at a time, and the duration should not exceed one second.

# Switching Characteristics at $V_{CC} = 5V$ and $T_A = 25^{\circ}C$

Symbol		R <sub>L</sub> =	$\mathbf{R_L} = 2 \ \mathbf{k}\Omega,$ $\mathbf{C_L} = 50 \ \mathbf{pF}$	
	Parameter	C <sub>L</sub> =		
		Min	Max	
t <sub>PLH</sub>	Propagation Delay		27	ns
t <sub>PHL</sub>	Data to Q		18	115
t <sub>PLH</sub>	Propagation Delay		36	ns
t <sub>PHL</sub>	LE to Q		25	115
t <sub>PZH</sub>	3-STATE Enable Time		20	ns
t <sub>PZL</sub>	OE to Q		25	ns
t <sub>PHZ</sub>	3-STATE Enable Time		20	ns
$t_{PLZ}$	OE to Q		25	115
t <sub>S</sub> (H)	Setup Time (HIGH/LOW)	3		ns
$t_S(L)$	Data to LE	7		115
t <sub>H</sub> (H)	Hold Time (HIGH/LOW)	10		ns
$t_H(L)$	Data to LE	10		115
t <sub>W</sub> (H)	Pulse Width (HIGH)	15		20
	Data to LE	15		ns



20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide Package Number M20B



20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide Package Number N20A

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