TOSHIBA MOS TYPE DEGITAL
INTEGRATED CIRCUIT
Silicon Monolithic CMOS Silicon Gate

TMP82C59AP-2/TMP82C59AM-2

PROGRAMMABLE INTERRUPT CONTROLLER

1. GENERAL DESCRIPTION

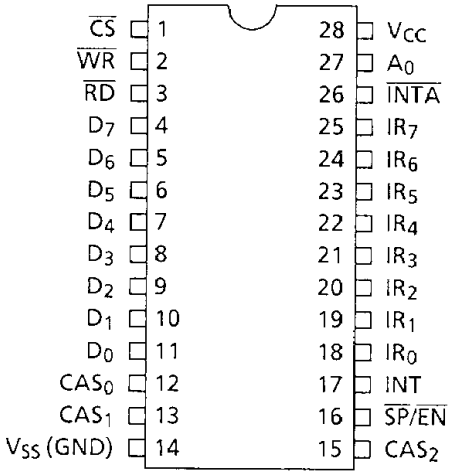
TMP82C59AP-2/AM-2 (hereinafter referred to as TMP82C59A) is a programmable interrupt controller. It handles up to eight vectored priority interrupts for the MPU. It is cascadable for up to 64 vectored priority interrupts without additional circuitry.

FEATURES

- Eight Level Priority Controller.
- Expandable to 64 Level.
- Interrupt Modes, Interrupt Mask, Vectored Address Programmable.
- Single +5V Power Supply.
- Supports 8085A, 8086 Microcomputer Interrupt Sequence.
- TTL Compatible.

2. PIN CONNECTIONS (TOP VIEW)

TMP82C59AP-2/TMP82C59AM-2



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3. PIN NAMES AND DESCRIPTION

Table 3.1

Pin Name	Input / Output	Function
$\overline{CS}$	Input	Chip Select Input. A low on this pin enables $\overline{RD}$ and $\overline{WR}$ communication between the MPU and the TMP82C59A. $\overline{INTA}$ functions are independent of $\overline{CS}$.
$\overline{WR}$	Input	Write Control Input. A low on this pin when $\overline{CS}$ is low enables the TMP82C59A to receive command words from MPU.
$\overline{RD}$	Input	Read Control Input. A low on this pin when $\overline{CS}$ is low enables the TMP82C59A to output status onto the data bus for the MPU.
D_0 to D_7	Input / Output	Bidirectional Data Bus. Command status and interrupt-vector information is transferred via this bus.
CAS_0 to CAS_2	Input / Output	Cascade Lines. The CAS lines from a private TMP82C59A bus to control a multiple TMP82C59A structure. These pins are outputs for a master TMP82C59A and inputs for a slave TMP82C59A.
$\overline{SP}$ / $\overline{EN}$	Input / Output	Slave Program / Enable buffer. This is a dual function pin. In the buffered mode, it can be used as an output to control buffer transceivers ($\overline{EN}$). In the non-buffered mode, it is used as an input to designate a master TMP82C59A ($\overline{SP} = 1$) or a slave one ($\overline{SP} = 0$).
INT	Output	Interrupt Request Output. This pin goes high whenever a valid interrupt request is asserted. It is used to interrupt the MPU. It is connected to MPU's interrupt pin.
IR_0 to IR_7	Input	Interrupt Request Inputs. An interrupt request is executed by raising an IR input (low to high), and holding it high until it is acknowledged (Edge Triggered Mode), or just by a high level on a IR input (Level Triggered Mode.)
$\overline{INTA}$	Input	Interrupt Acknowledge Input. This pin is used to output interrupt-vector data onto the data bus by a sequence of interrupt acknowledge pulses issued by the MPU.
A_0	Input	Address Line. This pin acts in conjunction with the $\overline{CS}$, $\overline{WR}$ and $\overline{RD}$ pins. It is used by the TMP82C59A to decipher various command words the MPU writes and status the MPU wishes to read. It is typically connected to the MPU A_0 address line.
VCC		+ 5V Power Supply
VSS		Ground

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4. FUNCTIONAL DESCRIPTION

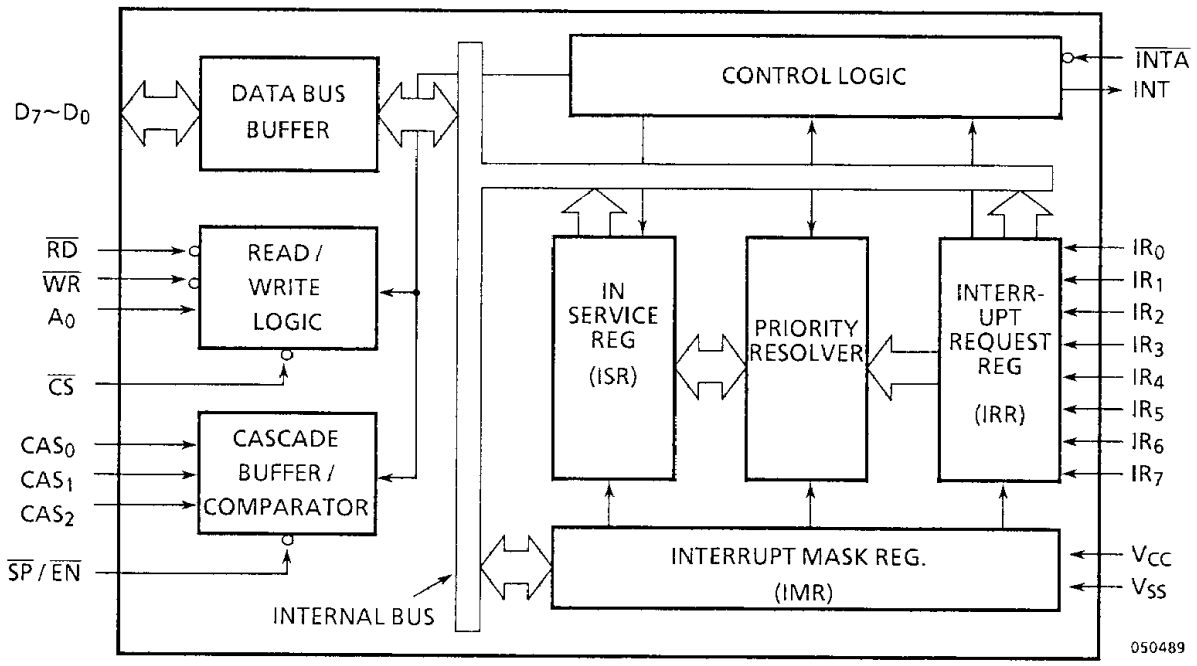

Figure 4.1 BLOCK DIAGRAM

The TMP82C59A is connected to the system bus as shown in Figure 4.2 and operates as an interrupt controller.

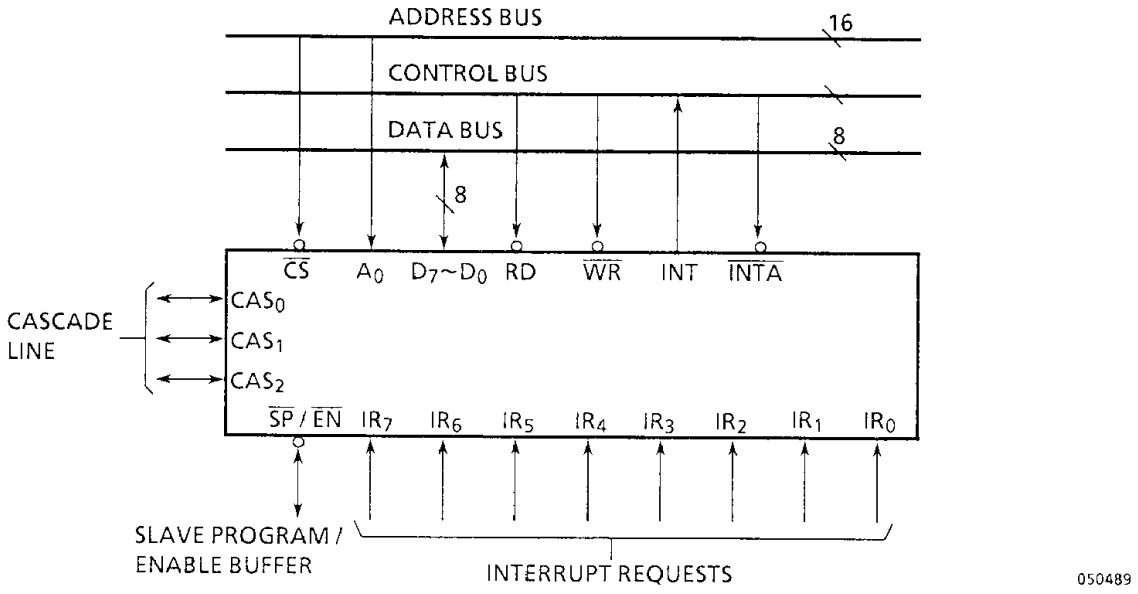

Figure 4.2 Interface to the System Bus

4.1 GENERAL DESCRIPTION

Whenever an interrupt request is received via IRn, the TMP82C59A, judging its mask status and priority, set INT high for requesting interrupt to MPU. Then, according to response signal ($\overline{INTA}$ signal) from MPU or the system controller, the TMP82C59A outputs CALL op-code and vectored address data on to the data bus. MPU starts the interrupt service routine and the TMP82C59A stores which interrupt request has been serviced. At the end of the service routine, MPU resets it and informs the TMP82C59A of its end.

Table 4.1 Basic Operation

A_0	D_4	D_3	$\overline{RD}$	$\overline{WR}$	$\overline{CS}$	READ OPERATION
0			0	1	0	IRR, ISR or Interrupt request level → Data bus
1			0	1	0	IMR → Data bus
A_0	D_4	D_3	$\overline{RD}$	$\overline{WR}$	$\overline{CS}$	WRITE OPERATION
0	0	0	1	0	0	Data bus → OCW2
0	0	1	1	0	0	Data bus → OCW3
0	1	×	1	0	0	Data bus → ICW1
1	×	×	1	0	0	Data bus → OCW1, ICW2, ICW3 or ICW4
A_0	D_4	D_3	$\overline{RD}$	$\overline{WR}$	$\overline{CS}$	HIGH IMPEDANCE
×	×	×	1	1	0	Data bus (D_7 to D_0) High impedance
×	×	×	×	×	1	Data bus (D_7 to D_0) High impedance

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4.2 SYSTEM CONFIGURATION

The TMP82C59A consists of the following components.

(1) Interrupt Request Register (IRR) and Inservice Register (ISR)

(2) Priority Resolver

(3) Interrupt Mask Register (IMR)

(4) Data Bus Buffer

(5) Read/Write Logic

(6) Cascade Buffer/Comparator

(7) Interrupt Request Register (IRR) and Inservice Register (ISR)

Interrupt requests from IRn inputs are processed by 2 registers, IRR and ISR. IRR holds interrupt request from the respective IRn inputs while ISR holds all interrupt levels that are being serviced by the MPU. Contents of IRR and ISR can be read out by the MPU.

(2) Priority Resolver

The priority resolver is the block that decides the interrupt request to be sent to MPU by judging priority. If the interrupt mask register (IMR) bit corresponding to IRn input is not set to 1, IRR sends the interrupt requests to the priority resolver.

Normally, when the interrupt request level having the highest priority among these interrupt request is higher than the content of ISR, that is, the priority of the interrupt request being serviced by the MPU, the TMP82C59A sends INT signal to the MPU. When $\overline{INTA}$ signal is input as a response from the MPU the TMP82C59A sends CALL op-code and the vectored address corresponding to an interrupt request of the highest priority to MPU, and resetting IRR bit corresponding to this interrupt request sets ISR bits. The MPU processes the interrupt service, sends a command to the TMP82C59A to accept interrupt requests of lower priority at the end of the interrupt service, and resets the corresponding ISR bits. The priority resolver has a register to assign the interrupt request input of lowest priority.

(3) Interrupt Mask Register (IMR)

The interrupt mask register normaly acts only on IRR, and disables interrupt requests from the masked IRn input. The mask for an interrupt request input does not affect its lower priority interrupt requests. In the special mask mode, this register also acts on ISR and enables acceptance of lower level interrupt requests than the interrupt request being serviced. The content of IMR can be read out.

(4) Data Bus Buffer

The data bus buffer consists of 8 bit 3 state bidirectional bus buffer interfacing with the system bus. Command words, status information CALL op-code and vectored addresses are transfered via this bus buffer.

(5) Read/Write Logic

This circuit controls the functions for decoding and accepting command words from MPU and for feeding status information to the data bus.
In addition, this circuit controls operations including ICW (Initialization Command Word) register and OCW (Operation Set Command Word) register.

$\overline{CS}$: Low level input to $\overline{CS}$ enables $\overline{RD}$ or $\overline{WR}$ input operation.

$\overline{WR}$: When $\overline{WR} = \overline{CS} = 0$, a command write to the TMP82C59A is enabled.

$\overline{RD}$: When $\overline{RD} = \overline{CS} = 0$, the contents of ISR, IRR and IMR and interrupt level in the poll mode can be read.

A_0 : A_0 is used together with $\overline{WR}$ and $\overline{RD}$ signals for command write or status readout. It acts as a select signal for the one of command words or status information. It is normally connected to the one of address lines.

(6) Cascade Buffer/Comparator

When programmed as a slave device, this block stores the identification code as the slave and compares this identification code with the data on the 3 bit cascade lines (CAS_{0-2}). When both agree, the slave interpretes that the slave itself is selected. In the case of the master, an identification signal corresponding to the accepted interrupt request inputs of the slave device are output for a period from the first $\overline{INTA}$ signal to the last $\overline{INTA}$ signal (second or third signal).

4.3 INTERRUPT SEQUENCE

(1) When the 8085A is used as the MPU

(a) When one or more interrupt request become high level, IRR bits corresponding to that input are set.

(b) The TMP82C59A judges the mask status and priority of these interrupt and outputs INT signal to MPU as necessary.

(c) MPU outputs $\overline{INTA}$ signal in response to INT signal.

(d) Upon receipt of $\overline{INTA}$ signal, the TMP82C59A outputs CALL op-code on the data bus.

(e) Since 'CALL' is a 3-byte instruction, additional two $\overline{INTA}$ signals are consecutively sent from MPU.

(f) Upon receipt of these two $\overline{INTA}$ signals, the TMP82C59A outputs the programmed vector address corresponding to the highest priority interrupt request. The TMP82C59A outputs the low-order address and then, the high-order address. Furthermore, the TMP82C59A sets the ISR bit corresponding to the interrupt request and resets IRR bit.

(g) The above operations complete CALL instruction and MPU executes the interrupt service. In AEOI mode, ISR bits are automatically reset immediately after the above operations. Otherwise, ISR bits are kept in the set status till EOI command is input.

(2) When the 8086 is used as MPU

(a) to (c) Same as (a) to (c) for the 8085A.

(d) Even when $\overline{INTA}$ signal is received, the TMP82C59A keeps the data bus in high impedance state.

(e) Another $\overline{INTA}$ signal is sent from MPU. The TMP82C59A outputs 8 bit pointer on the data bus, and sets the corresponding ISR bit and resets the IRR bit.

(f) The above operations complete the interrupt acknowledge cycle. In AEOI mode, the ISR bit is automatically reset after the final $\overline{INTA}$ signal is received. Otherwise, ISR bits are kept in the set status till EOI command is input.

Further, if there is no interrupt request at the time of step (d) of the above interrupt sequence, (i.e., the request was too short in duration), the TMP82C59A performs the same operations as those when interrupt request are generated at IR_7, but ISR bits are not set.

4.4 INTERRUPT SEQUENCE OUTPUT

(1) When the 8085A is used as the MPU

CALL op-code is output on the data bus upon receipt of the first $\overline{INTA}$ signal and the low-order vectored address and the high-order vectored address on the data bus upon receipt of the second and third $\overline{INTA}$ signals, respectively.

The vectored address A_5 to A_{15} on Table 4.3, 4.4 must be programmed in advance on the TMP82C59A. The remaining bits of the vectored addresses are produced by the TMP82C59A corresponding to interrupt request.

(2) When the 8086 is used as the MPU

When the first $\overline{INTA}$ signal is received, the data bus is placed in the high impedance state. When the second $\overline{INTA}$ signals is received, 8 bit pointer is output on the data bus. The 8 bit pointers T_7 to T_3 shown in Table 4.5 must be programmed in advance on the TMP82C59A. The remaining bits are automatically produced by the TMP82C59A corresponding to interrupts.

(1) 8085A MODE

Table 4.2 For First $\overline{INTA}$

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	1	0	0	1	1	0	1

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Table 4.3 For Second $\overline{INTA}$

IR	INTERVAL = 4							
	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
IR_7	A_7	A_6	A_5	1	1	1	0	0
IR_6	A_7	A_6	A_5	1	1	0	0	0
IR_5	A_7	A_6	A_5	1	0	1	0	0
IR_4	A_7	A_6	A_5	1	0	0	0	0
IR_3	A_7	A_6	A_5	0	1	1	0	0
IR_2	A_7	A_6	A_5	0	1	0	0	0
IR_1	A_7	A_6	A_5	0	0	1	0	0
IR_0	A_7	A_6	A_5	0	0	0	0	0

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IR	INTERVAL = 8							
	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
IR_7	A_7	A_6	1	1	1	0	0	0
IR_6	A_7	A_6	1	1	0	0	0	0
IR_5	A_7	A_6	1	0	1	0	0	0
IR_4	A_7	A_6	1	0	0	0	0	0
IR_3	A_7	A_6	0	1	1	0	0	0
IR_2	A_7	A_6	0	1	0	0	0	0
IR_1	A_7	A_6	0	0	1	0	0	0
IR_0	A_7	A_6	0	0	0	0	0	0

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Table 4.2 For Third $\overline{INTA}$

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
A_{15}	A_{14}	A_{13}	A_{12}	A_{11}	A_{10}	A_9	A_8

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(2) 8086 MODE

Table 4.5 Second $\overline{INTA}$

	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
IR_7	T_7	T_6	T_5	T_4	T_3	1	1	1
IR_6	T_7	T_6	T_5	T_4	T_3	1	1	0
IR_5	T_7	T_6	T_5	T_4	T_3	1	0	1
IR_4	T_7	T_6	T_5	T_4	T_3	1	0	0
IR_3	T_7	T_6	T_5	T_4	T_3	0	1	1
IR_2	T_7	T_6	T_5	T_4	T_3	0	1	0
IR_1	T_7	T_6	T_5	T_4	T_3	0	0	1
IR_0	T_7	T_6	T_5	T_4	T_3	0	0	0

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4.5 PROGRAMMING TMP82C59A

The TMP82C59A accepts the following 2 types of command words.

(1) Initialization Command Words (ICW)

Prior to operating the TMP82C59A, it is necessary to program this command.

(2) Operation Command Words (OCW)

This command is for operating the TMP82C59A in various operating modes and is programmable anytime during the TMP82C59A is in operation.

(1) ICW

There are 4 kinds of commands; ICW1, ICW2, ICW3 and ICW4.
Each of these command is not programmable independently. The initialization is made according to the initialization command sequence shown in Figure 4.3. ICW3 is used for cascade connection and ICW4 is for setting optional modes.

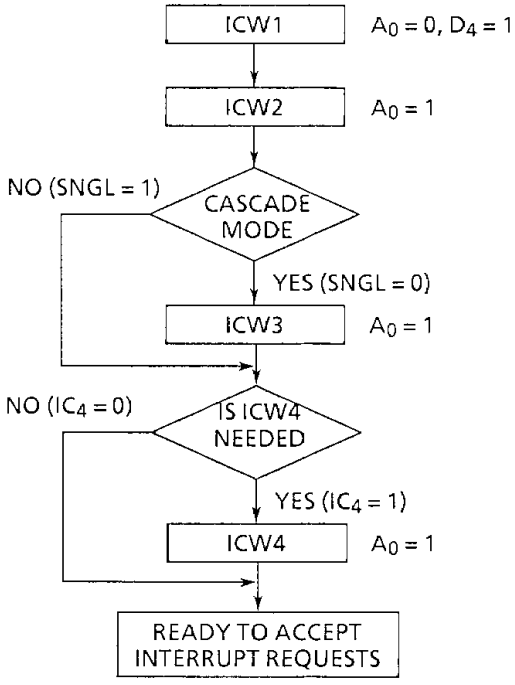


Figure 4.3 Initialization Command Sequence

ICW1

When $A_0=0$ and $D_4=1$, the initialization is interpreted as ICW1 and the initialization of following 5 items are made independently of content of the command:

[1] The interrupt mask register (IMR) is cleared.

[2] The interrupt request input IR_7 becomes the lowest priority.

[3] The special mask mode is cleared and IRR is assigned as the register for reading status information.

[4] When $IC_4=0$, all function bits of ICW4 are set at "0".

[5] The edge detection circuit of the interrupt request terminal is cleared.

ICW1 makes the assignment of vector addresses A_7 to A_5, assignment as to whether the interrupt request input is to be made in the edge trigger mode or the level trigger mode (LTIM), assignment of CALL address intervals when the 8085A is used as MPU (refer to Table 4.3) (ADI), assignment as to whether the cascade connection to be made (SNGL) and assignment as to whether ICW4 is needed (IC4).

ICW2

ICW2 assigns high-order vector addresses A_8 to A_{15} when the 8085A is used as MPU or 8-bit pointers T_3 to T_7 when the 8086 is used as MPU. TMP82C59A interpretes a command written with A_0 input made to "H" level after ICW1 written as ICW2.

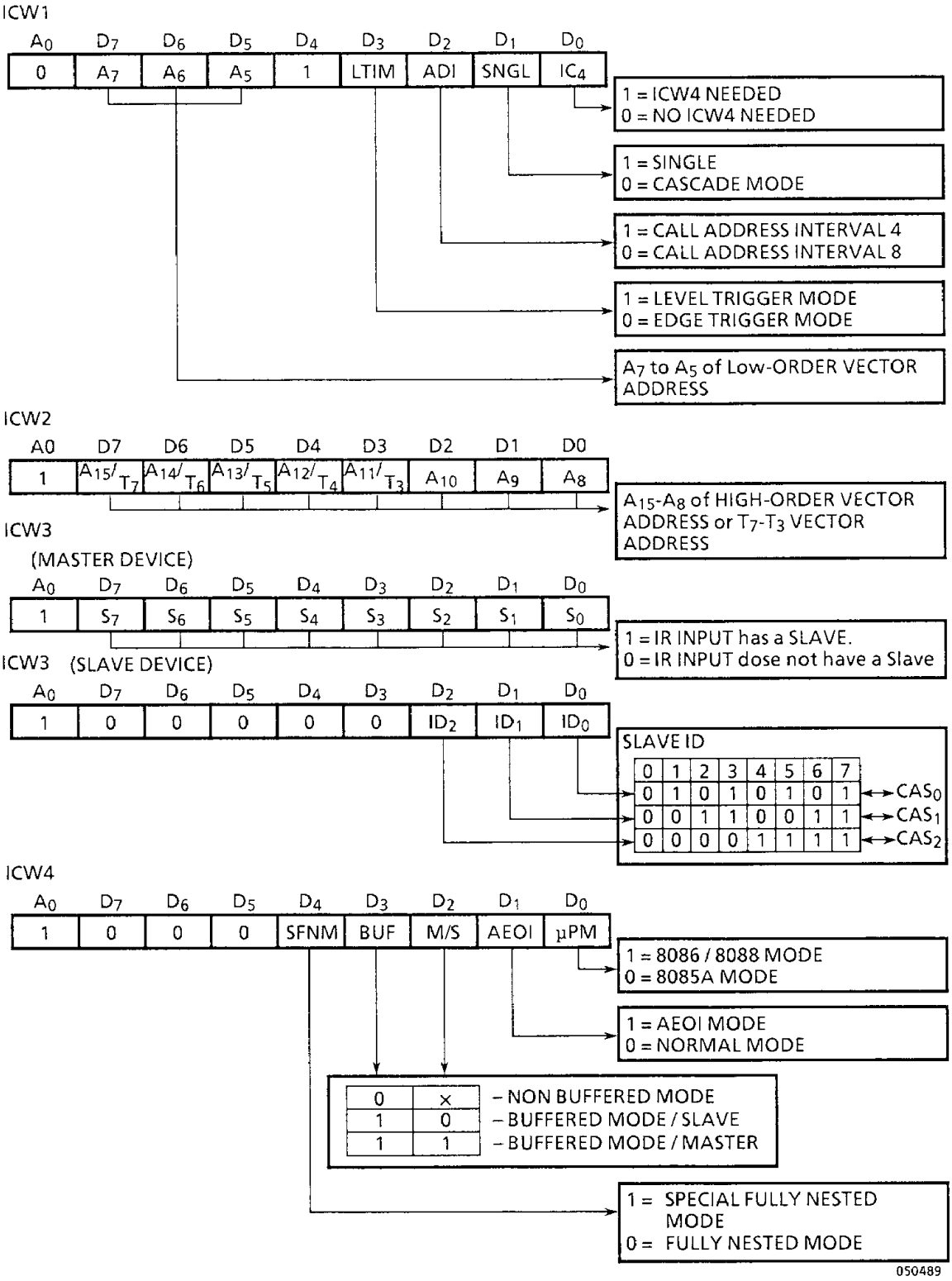


Figure 4.4 ICW Format

ICW3

This is a command required for cascade connection of plural number of the TMP82C59As. When SNGL = 0 in ICW1, the TMP82C59A interpretes a command written with A_0 input made at "H" level after ICW2 as ICW3.

[1] Master Mode

In the master mode, the TMP82C59A specifies individually as to whether a slave device is added to each interrupt request input.
If the 8085A is used as MPU when addition of a slave device is specified, the master device outputs CALL op-code on the data bus upon receipt of the first $\overline{INTA}$ signal and simultaneously outputs the slave identification code to the cascade line.

The master device becomes high impedance at the second and third $\overline{INTA}$ signals, and the slave devices selected by the identification code outputs vector address on the data bus. When the 8086 is used as MPU, both the master and slave devices become high impedance at the first $\overline{INTA}$ signal. Simultaneously, the master device outputs the slave identification code to the cascade line. The master device also become high impendance at the second $\overline{INTA}$ signal and the selected slave device outputs a pointer on the data bus. When it is specified that no slave device is added, the master device outputs both CALL op-code and vector address as a response to $\overline{INTA}$ signal and simultaneously outputs "L" signal to 3 cascade lines. This is the same as the identification code of the slave device connected to IR_0 and therefore, in the case of the interrupt request input without the slave device, added, no slave device can be added to IR_0.

Further, to specify the master or slave, the $\overline{SP}/\overline{EN}$ terminal must be set at "H" level or BUF must be set at 1 and M/S at 1 by ICW4.

[2] Slave Mode

In the slave mode, the TMP82C59A specifies the slave identification code.
The slave device compares its identification code with the identification code sent from the master device via the cascade line and if they agree, outputs vector addresses on the data bus upon receipt of the second and third $\overline{INTA}$ signals.
Further, to specify the slave mode, the $\overline{SP}/\overline{EN}$ terminal must be set at "L" level or BUF at 1 and M/S at 0 by ICW4.

ICW4

ICW4 is effective only when $IC_4 = 1$ in ICW1.
Although ICW4 is effective for assignment of the special fully nested mode (SFNM), assignment of the buffer mode (BUF) and in the buffer mode, this command makes the assignment of the master/slave (M/S), automatic EOI (AEOI) and MPU mode. When $IC_4 = 0$ in ICW1, all function bits of ICW4 are set at "0".

(2) OCW

There are 3 kinds of commands: OCW1, OCW2, and OCW3. Any time after ICW is programmed, these command can be programmed to set the TMP82C59A in various operation modes.

OCW1

After ICW is set, the TMP82C59A interpretes the operation set command to be OCW1when $A_0 = 1$. This command is used for setting the content of the interrupt mask register (IMR). The OCW1 format is shown in Figure 4.5.

OCW2

The TMP82C59A interpretes the operation set command to be OCW2 when $A_0 = 0$, $D_4 = 0$ and $D_3 = 0$. This command is used for outputting EOI. L_2 to L_0 are effective only in the case of specific EOI and specific rotation.
The OCW2 format is shown in Figure 4.5.

OCW3

The TMP82C59A interpretes the operation set command to be OCW3 when $A_0 = 0$, $D_4 = 0$ and $D_3 = 1$. This command is used for assigning the special mask mode, the poll mode and register for status information readout, that is, assigning IRR or ISR. The OCW3 format is shown in Figure 4.5.

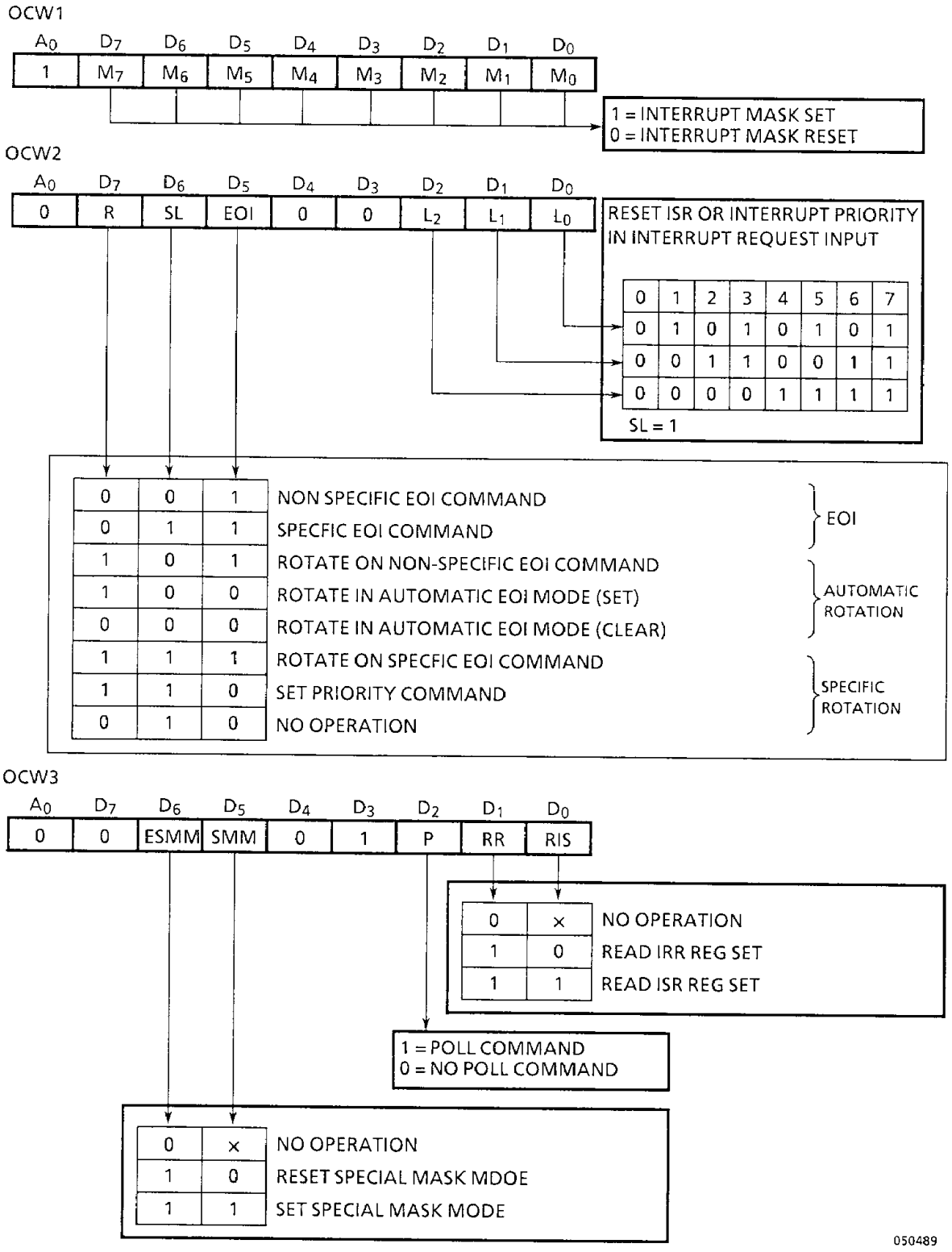


Figure 4.5 OCW Format

4.6 EXPLANATION OF MODES AND COMMANDS

(1) FULLY NESTED MODE

Unless the other modes are specified, the TMP82C59A operates in this mode. Under this mode, IR_0 is the highest priority level and IR7 bocomes the lowest.

When $\overline{INTA}$ signal is input, vector address corresponding to an interrupt and request having the highest priority at the time is output together with CALL op-code on the data bus and furthermore, corresponding ISR bits are kept set till EOI command is input to the TMP82C59A before MPU returns from the service routine or to the final leading edge of $\overline{INTA}$ pulse in AEOI mode. As long as these ISR bits are kept set, lower priority interrupt requests are ignored. Priority can be changed by OCW2.

(2) EOI (END OF INTERRUPT)

EOI command is used to reset ISR bits. It is necessary for MPU to output EOI command before returning from the service routine.

When AEOI is set in ICW4, ISR bit are automatically reset at the leading edge of the final $\overline{INTA}$ pulse and it is therfore not necessary to output EOI command. As ISR bits are set in both the master and slave devices when cascade connected, it is necessary to output EOI command to both master device and the slave device corresponding to the master device.

EOI command is available in 2 kinds: non-specific EOI and specific EOI commands. When non-specific EOI command is output to the TMP82C59A, ISR bit having the highest priority among ISR bit is reset. However, in the special mask mode it is not possible to reset ISR bit that are masked by IMR by the non-specific EOI command, and ISR bit having the highest priority among the unmasked ISR bits is reset. On the other hand, it is possible to specify ISR bit to be reset by the specific EOI command by a program. EOI command is executed by OCW2.

(3) AEOI (AUTOMATIC EOI) MODE

In this mode, the non-specific EOI operation is automatically executed at the leading edge of the final $\overline{INTA}$ signal.

Therefore, this mode cannot be used for nested interruptions. In addition, this mode also cannot be used in the slave TMP82C59A. The TMP82C59A can be set in AEOI mode by setting AEOI bit in ICW4 to 1.

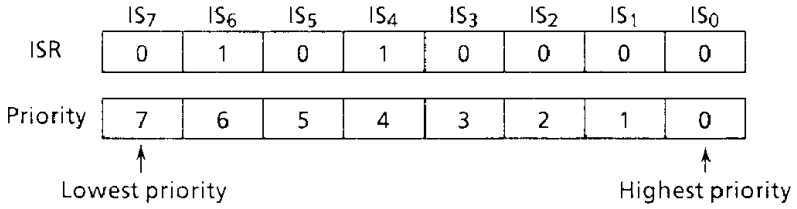
(4) AUTOMATIC ROTATION

This mode is effective in the application to give equal priority to the interrupt devices. In this mode, whenever the interrupt service ends, priority of each interrupt request is updated so that the serviced interrupt request is set at the lowest priority. Priority of interrupt request input IRn (n=0 to 7) that has been serviced becomes the lowest priority level 7 and becomes high in order toward IR_0 and then, IR_7 and next IR_{n+1} become the highest priority level 0. (Rotation Priority)

For instance, when the interrupt request IR_4 is seviced as shown in Figure 4.6, the priority of each interrupt request input is updated.

This mode specifies R=1, SL=0 and EOI=1 by OCW2 at the end of service. Further, in case of AEOI mode, when R=1, SL=0 and EOI=0 are specified by OCW2, the internal flip-flop is set and the TMP82C59A operates in this mode. If R=0, SL=0 and EOI=0 are specified by OCW2, this mode is cleared.

before Rotation (highest priority interrupt request IR_4 is being serviced.)



After ROTATION (Interrupt request IR_4 is being serviced.)

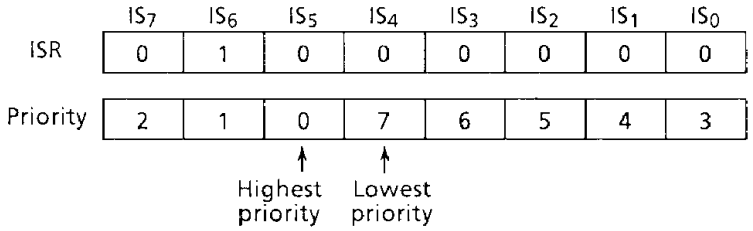


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Figure 4.6 The Example of Interrupt Priority Transition in Automatic Rotation Mode

(5) SPECIFIC ROTATION

In the automatic rotation mode, priority of each interrupt request input is updated whenever interrupt requests are serviced. Under this mode it is possible to change priority by specifying an interrupt request input to be set at the lowest priority by a program. Priority is determined according to the ratation priority. In this mode, R and SL are set at 1 by OCW2 and interrupt request input that is to be lowest priority at L_2 to L_0 is specified. Priority can be changed simultaneously with EOI command or independently regardless of EOI command.

(6) INTERRUPT MASK

Each interrupt request input can be masked individually by the interrupt mask register (IMR). Content of IMR can be specified by OCWI.

(7) SPECIAL MASK MODE

Normally when an interrupt service routine is being executed, lower priority interrupt requests than the interrupt request being serviced are ignored unless ISR bits are reset by EOI command. This special mode is used for an application in which an interrupt request of lower priority is approved during the service. In this mode, IMR also acts as the mask for ISR. That is, the TMP82C59A processes an interrupt request by assuming that ISR bit and IRR bit corresponding to IMR bit set at "1" have not been set. This mode is set by setting ESMM = 1 and SMM = 1 by OCW3.

Further, when ESMM = 1 and SMM = 0 are assigned by OCW3, this mode is cleared to the normal mode. The IMR programming is made by OCW1.

(8) POLL COMMAND

This mode is used in a state where the internal interrupt enable flip-flop of MPU is disabled and no interrupt is authorized. The service to the device is made by using the poll command. The poll command specifies P = 1 in OCW3. The mode becomes now the poll mode. When the read operation ($\overline{RD}$ = 0, $\overline{CS}$ = 0) is made on the TMP82C59A, the following output is made on the data bus:

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
I	–	–	–	–	W_2	W_1	W_0

W_0~W_2 : Binary code of highest priority interrupt request among interrupt requests to the interrupt request inputs.

I : There is an interrupt request to MPU when I = 1.

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Figure 4.7 Poll Mode Data Format

The TMP82C59A interpretes $\overline{RD}$ signal as the interrupt acknowledge and when D_7 = 1 is output, sets corresponding ISR bit. This poll mode is valid for a period from $\overline{WR}$ (P = 1 in OCW3) to next $\overline{RD}$ ($\overline{CS}$ = 0). Further, an interrupt request to be serviced is determined at the time when the mode is made to the poll mode and end even when a new or high priority interrupt request is sent between $\overline{WR}$ and $\overline{RD}$, it is not accepted.

(9) READING STATUS

MPU is capable of reading the contents of 3 registers (IRR, ISR, IMR). When the reading operation is made at $A_0 = 0$, the content of IRR or ISR can be read out. Selection of IRR and ISR is made by OCW3. When RR is set at 1 and RIS at 0, IRR is assigned and when RR and RIS are set at 1, ISR is assigned.

This assignment is kept stored without necessity for performing at every reading operation. IMR is read when $A_0 = 1$. If the poll mode is specified before the reading operation, the poll command has priority.

(10) EDGE TRIGGERED MODE / LEVEL TRIGGERED MODE

This mode is selected by LTIM of ICWI.

When LTIM is 0, the edge triggered mode is selected and interrupt request is triggered at the leading edge of the interrupt request signal and kept continued by holding "H" level. When LTIM is 1, the level triggered mode is selected and interrupt request is recognized by "H" level of the interrupt request signal. For both modes it is necessary to hold the interrupt request input at "H" level by triggering it till the fast $\overline{INTA}$ signal is output from MPU. If the interrupt request input is at "L" level when $\overline{INTA}$ signal is output from MPU, the same operations as those when interrupt requests are generated at IR_7 are performed but ISR bits are not set.

(11) SPECIAL FULLY NESTED MODE

This mode is used to give priority to the interrupt request input for the slave devices when they are cascade connected.

This mode is assigned to the master TMP82C59A when SFNM is 1 in ICW4.

With the exception of the following 2 points, this mode is identical to the fully nested mode.

[1] Even when an interrupt request from a slave device is being serviced, the master device accepts a higher priority interrupt request from the same slave device without ignoring it. (In the fully nested mode, a higher priority interrupt request from the slave device that is now being serviced is ignored and interrupt requests from a higher priority slave device only are accepted.)

[2] When an interrupt request from a slave device is being serviced, it is necessary to check by a software as to whether the interrupt request is only one interrupt request from that slave device.

When the service ended, after the non-specific EOI is output to that slave device, MPU has to check whether all ISR bits of that slave device are "0". If they are all "0", that slave has no interrupt request being serviced and therefore, the non-specific EOI is output to the master device to allow acceptance of interrupt request from the lower priority slave devices.

Otherwise, the non-specific EOI must not be output to the master device.

(12) BUFFERED MODE

This mode is to output an enable signal to a data bus buffer from the $\overline{SP}/\overline{EN}$ terminal when the data bus buffer is needed for the data bus on a large system. Under this mode, "L" level signal is output to the $\overline{SP}/\overline{EN}$ terminal whenever the data bus output of the TMP82C59A is enabled. The assignment of this mode is made by ICW4 simultaneously with the assignment of the master/slave devices.

(13) CASCADE MODE

The TMP82C59A is able to process interrupt requests up to 64 levels by one master and 8 slave devices.

The cascading is shown in Figure 4.8. The master TMP82C59A selects the slave devices by the identification codes fully using 3 cascade lines. INT output of each slave device is connected to the interrupt request inputs of the master device. Further, the identification codes corresponding to respective connections are assigned for the slave devices by ICW3.

When interrupt request are generated at the interrupt request inputs of the slave devices and accepted, the master device outputs the identification code to the slave device at the first $\overline{INTA}$ signal trailing edge to output vector address or pointer. This identification code is kept maintained to the leading edge of the final $\overline{INTA}$ signal. Normally, the master device outputs "L" level signal to all cascade line. EOI command must be output twice; to the master and second, to the slave corresponding to the interrupt service. Further, an address decoder is required to activate to the $\overline{CS}$ input of each TMP82C59A.

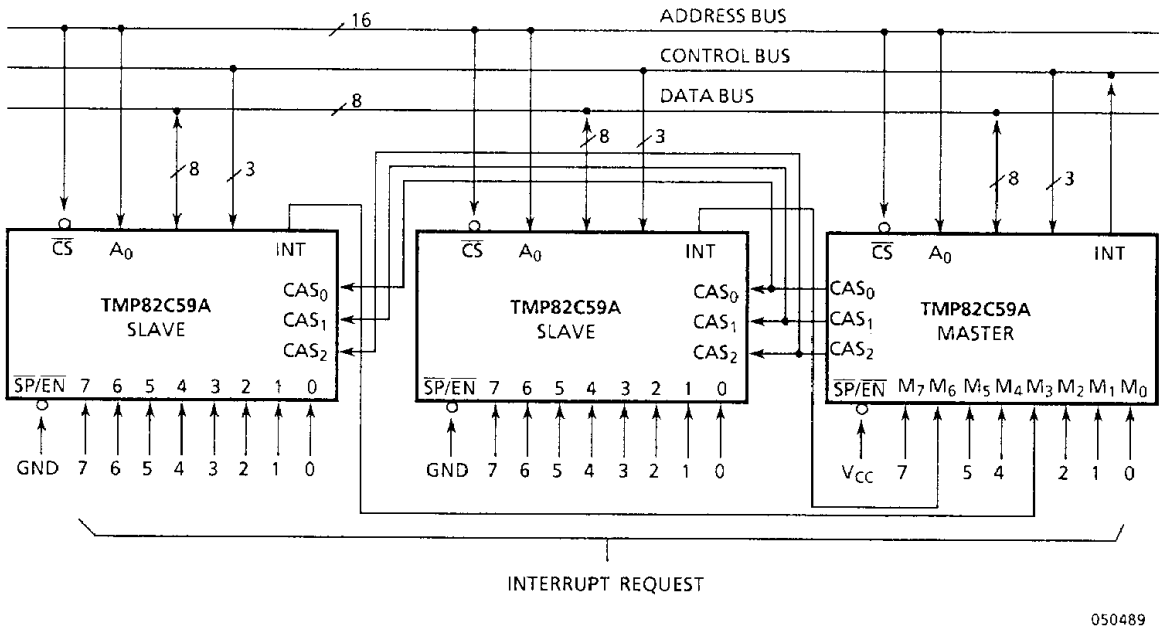

Figure 4.8 CASCADING

5.1 ABSOLUTE MAXIMUM RATINGS

SYMBOL	ITEM	RATING
VCC	VCC Supply Voltage (with respect to VSS (GND))	-0.5 to +7V
VIN	Input Voltage	-0.5 to V_{CC} + 0.5V
VOUT	Output Voltage	-0.5 to V_{CC} + 0.5V
PD	Power Dissipation	250mW
Tsol	Soldering Temperature (Soldering Time 10 sec)	260℃
Tstg	Storage Temperature	-65℃ to +150℃
Topr	Operating Temperature	-40℃ to +85℃

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5.2 DC CHARACTERISTICS

Ta = −40 to +85°C, VCC = 5 ± 10%, Vss (GND) = 0V, Unless otherwise noted.

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
VIL	Input Low Voltage		-0.5	—	0.8	V
VIH	Input High Voltage		2.2	—	VCC + 0.5	V
VOL	Output Low Voltage	IOL = 2.2mA	—	—	0.45	V
VOH1	Output High Voltage	IOH1 = -400μA	2.4	—	—	V
VOH2	Output High Voltage	IOH2 = -100μA	VCC-0.8	—	—	V
IIL	Input Leak Current	0V ≦ VIN ≦ VCC	—	—	± 10	μA
IIOFL	Output Leak Current	0.45V ≦ VIN ≦ VCC	—	—	± 10	μA
ILIR	Input Current (IR)	VIN = 0V	—	—	-300	μA
		VIN = VCC	—	—	10	μA
ICC1	Operating Supply Current	I / O CYCLE = 1μS VIH = VCC-0.2V VIH = 0.2V	—	—	5	mA
ICC2	Stand-by Supply Current	VIH = VCC-0.2V VIL = 0.2V	—	—	10	μA

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5.3 INPUT CAPACITANCE

Ta = 25°C, VCC = VSS (GND) = 0V

SYMBOL	PARAMETER	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
CIN	INPUT CAPACITANCE	fC = 1 MHz Unmeasured pins, 0V	—	—	10	pF
CI / O	INPUT / OUTPUT CAPACITANCE		—	—	20	pF

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5.4 AC CHARACTERISTICS

Ta = −40°C to +85°C, VCC = 5V ± 10%, VSS (GND) = 0V

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
TAHRL	A_0 / $\overline{CS}$ Setup Time ($\overline{RD}$)		0	—	—	ns
TRHAX	A_0 / $\overline{CS}$ Hold Time ($\overline{RD}$)		0	—	—	ns
TRLRH	$\overline{RD}$ Pulse Width		160	—	—	ns
TAHWL	A_0 / $\overline{CS}$ Setup Time ($\overline{WR}$)		0	—	—	ns
TWHAX	A_0 / $\overline{CS}$ Hold Time ($\overline{WR}$)		0	—	—	ns
TWLWH	$\overline{WR}$ Pulse Width		120	—	—	ns
TDVWH	D_0 to D_7 Setup Time ($\overline{WR}$)		120	—	—	ns
TWHDX	D_0 to D_7 Hold Time ($\overline{WR}$)		0	—	—	ns
TJLJH	Input IR Low Level Pulse width (Edge Trigger Mode)		100	—	—	ns
TCVIAL	Casecade Setup Time (Second or Third $\overline{INTA}$)		40	—	—	ns
TRHRL	$\overline{RD}$ to Next Command		160	—	—	ns
TWHWL	$\overline{WR}$ to Next Command		190	—	—	ns
TCHCL	End of Command to next Command (Not Same)		250	—	—	ns
	End of $\overline{INTA}$ sequence to next $\overline{INTA}$ sequence					
TRLDV	Valid Data Delay ($\overline{RD}$ / $\overline{INTA}$)	D_7 to D_0 CL = 100pF	—	—	120	ns
TRHDZ	Data Floating ($\overline{RD}$ / $\overline{INTA}$)		10	—	85	ns
TJHIH	Interrupt Output Delay (IR)	INT CL = 100pF	—	—	300	ns
TIALCV	Valid Cascade Delay ($\overline{INTA}$)		—	—	360	ns
TRLEL	Enable Active ($\overline{RD}$ / $\overline{INTA}$)	CAS_0 to 2 CL = 100pF	—	—	100	ns
TRHEH	Enable Inactive ($\overline{RD}$ / $\overline{INTA}$)		—	—	150	ns
TAHDV	Valid Data Delay (A_0 / $\overline{CS}$)		—	—	200	ns
TCVDV	Valid Data Delay (CAS_0 to CAS_2)		—	—	200	ns

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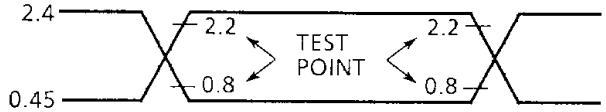
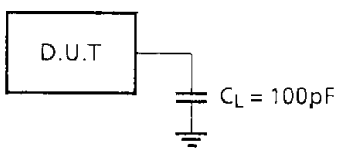
AC CHARACTERISTICS TEST CONDITION

AC Testing I / O Waveform



AC Testing Load Circuit



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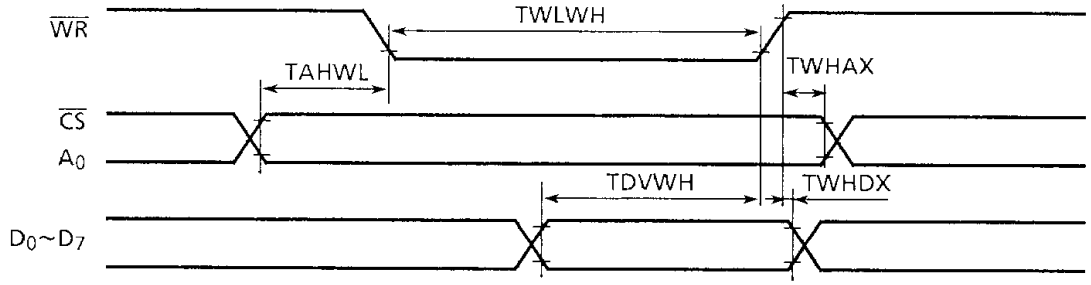
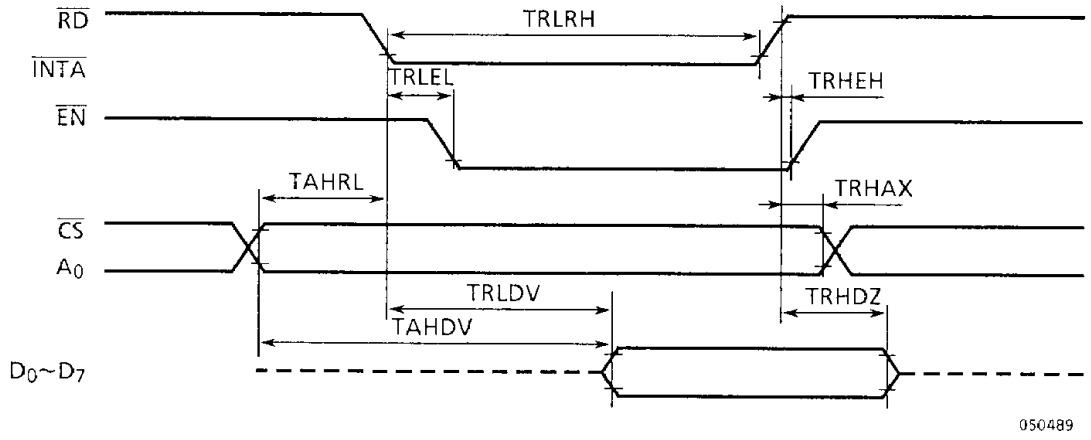
6. TIMING WAVEFORMS

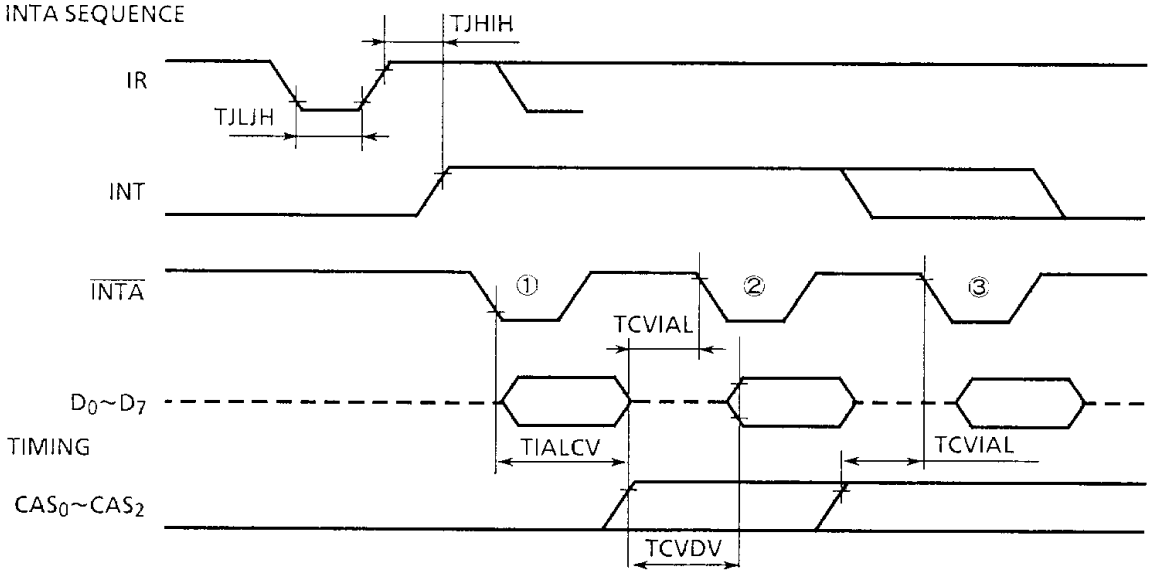
WRITE OPERATION



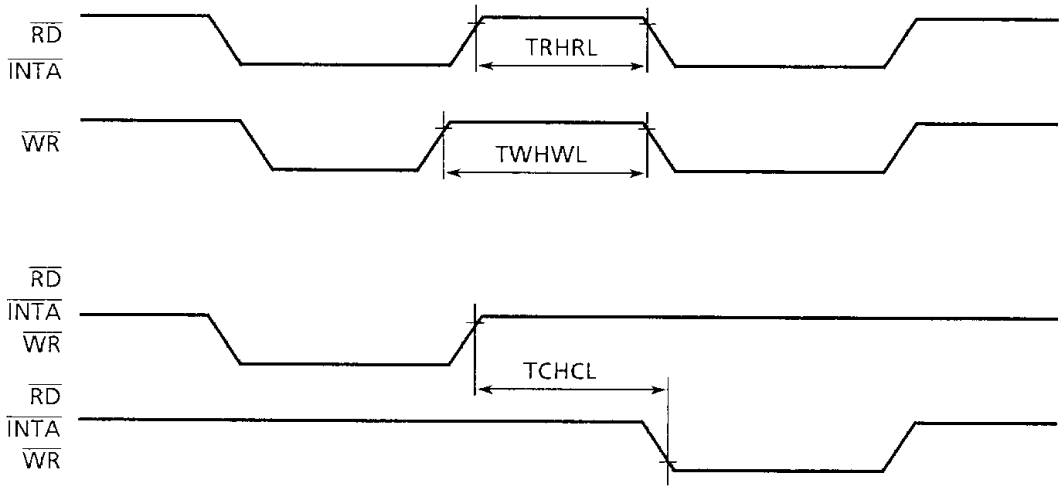
READ AND INTA OPERATION



INTA SEQUENCE



OTHER TIMING



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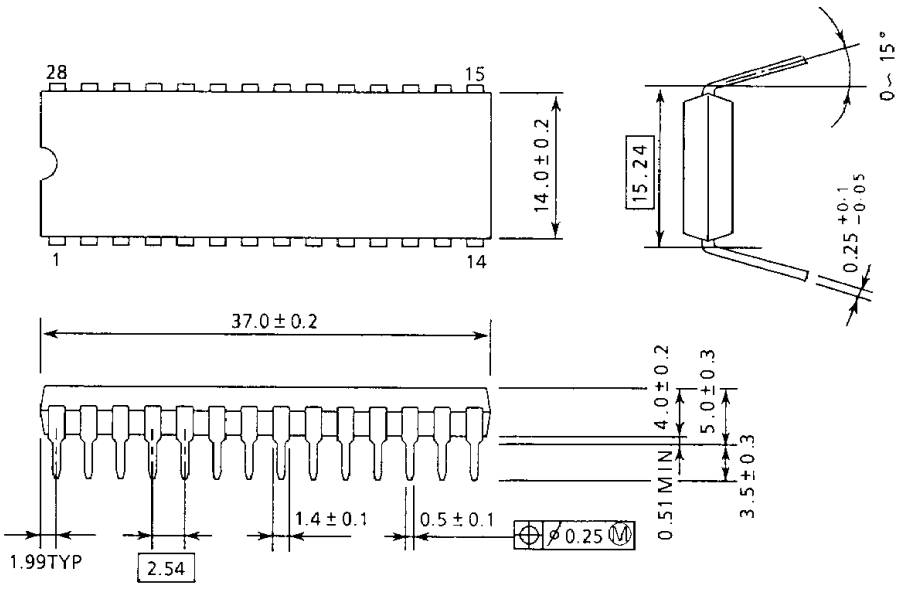
7. EXTERNAL DIMENSION VIEW

7.1 28 pins PRASTIC DIP

DIP28-P-600

Unit : mm



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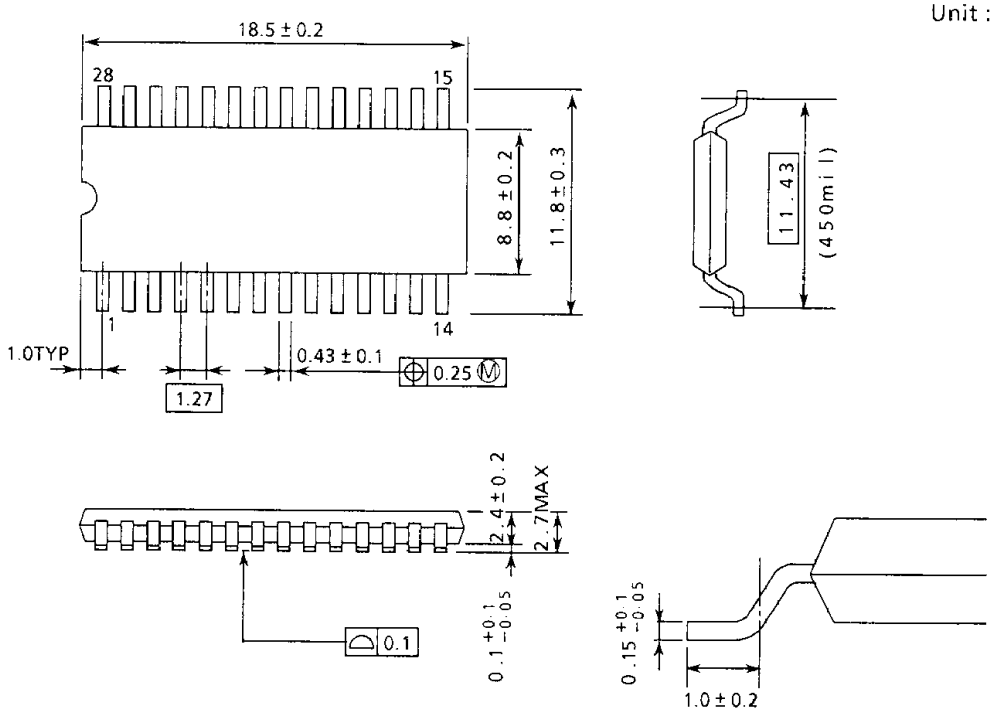
Note : Each lead pitch is 2.54mm, and all the leads are located within ±0.25mm from their theoretical position with respect to NO. 1 and NO. 28 leads.

7.2 28 pins SMALL OUTLINE PACKAGE

SOP28-P-450

Unit : mm



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Note : Package Width and Length do not include Mold Protrusions.
Allowable Mold Protrusion is 0.15mm.