CD405xB CMOS Single 8-Channel Analog Multiplexer/Demultiplexer with Logic-Level Conversion

1 Features

- Wide Range of Digital and Analog Signal Levels
  - Digital: 3 V to 20 V
  - Analog: ≤ 20 V_{P-P}
- Low ON Resistance, 125 Ω (Typical) Over 15 V_{P-P} Signal Input Range for $V_{DD} – V_{EE}$ = 18 V
- High OFF Resistance, Channel Leakage of ±100 pA (Typical) at $V_{DD} – V_{EE}$ = 18 V
- Logic-Level Conversion for Digital Addressing Signals of 3 V to 20 V ($V_{DD} – V_{SS}$ = 3 V to 20 V) to Switch Analog Signals to 20 V_{P-P} ($V_{DD} – V_{EE}$ = 20 V) Matched Switch Characteristics, r_{ON} = 5 Ω (Typical) for $V_{DD} – V_{EE}$ = 15 V Very Low Quiescent Power Dissipation Under All Digital-Control Input and Supply Conditions, 0.2 µW (Typical) at $V_{DD} – V_{SS} = V_{DD} – V_{EE}$ = 10 V
- Binary Address Decoding on Chip
- 5 V, 10 V, and 15 V Parametric Ratings
- 100% Tested for Quiescent Current at 20 V
- Maximum Input Current of 1 µA at 18 V Over Full Package Temperature Range, 100 nA at 18 V and 25°C
- Break-Before-Make Switching Eliminates Channel Overlap

2 Applications

- Analog and Digital Multiplexing and Demultiplexing
- A/D and D/A Conversion
- Signal Gating
- Factory Automation
- Televisions
- Appliances
- Consumer Audio
- Programmable Logic Circuits
- Sensors

3 Description

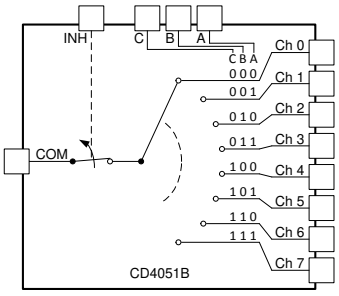
The CD405xB analog multiplexers and demultiplexers are digitally-controlled analog switches having low ON impedance and very low OFF leakage current. These multiplexer circuits dissipate extremely low quiescent power over the full $V_{DD} – V_{SS}$ and $V_{DD} – V_{EE}$ supply-voltage ranges, independent of the logic state of the control signals.

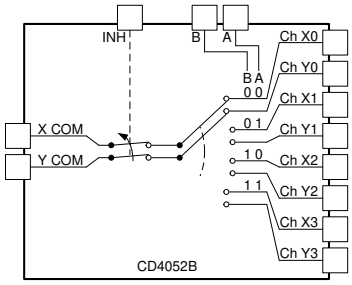
Device Information(1)

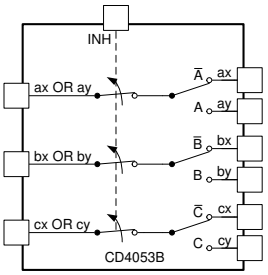
PART NUMBER	PACKAGE	BODY SIZE (NOM)
CD405xB	CDIP (16)	19.50 mm × 6.92 mm
	PDIP (16)	19.30 mm × 6.35 mm
	SOIC (16)	9.90 mm × 3.91 mm
	SOP (16)	10.30 mm × 5.30 mm
	TSSOP (16)	5.00 mm × 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Functional Diagrams of CD405xB







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4 Revision History

Changes from Revision H (April 2015) to Revision I **Page**

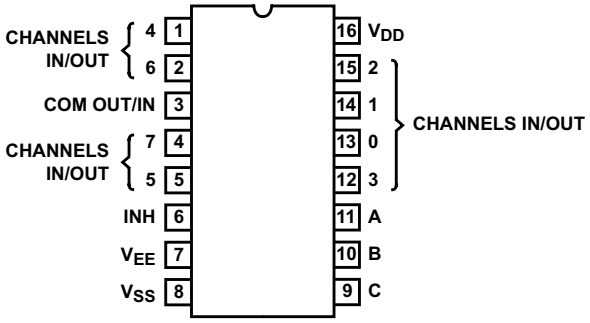
- Added: ON Channel Leakage Current to the *Electrical Characteristics* table ... 6
- Added Note 3 to the *Electrical Characteristics* table ... 6
- Added Figure 13 ... 11

Changes from Revision G (October 2003) to Revision H **Page**

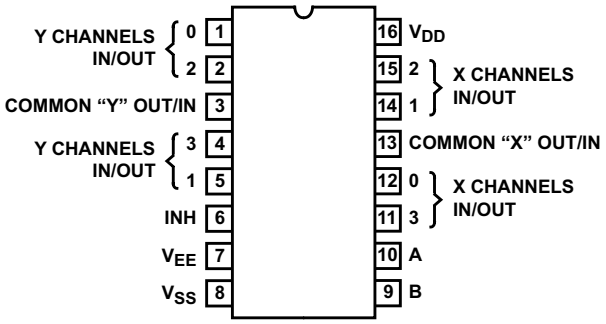
- Added *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1
- Added *Device Information* table. ... 1

5 Pin Configuration and Functions

CD4051B E, M, NS, and PW Package
16-Pin PDIP, CDIP, SOIC, SOP, and TSSOP
(Top View)



CD4052B E, M, NS, and PW Package
16-Pin PDIP, CDIP, SOP, and TSSOP
(Top View)



CD4053B E, M, NS, and PW Package
16-Pin PDIP, CDIP, SOP, and TSSOP
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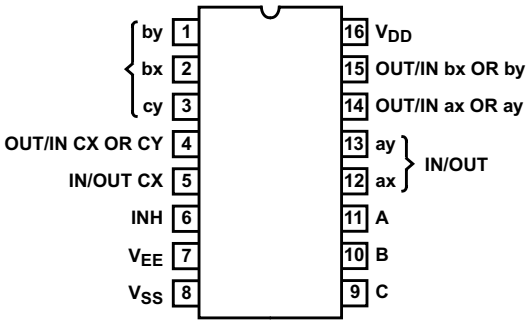


Pin Functions CD4051B

PIN		I/O	DESCRIPTION
NO.	NAME		
1	CH 4 IN/OUT	I/O	Channel 4 in/out
2	CH 6 IN/OUT	I/O	Channel 6 in/out
3	COM OUT/IN	I/O	Common out/in
4	CH 7 IN/OUT	I/O	Channel 7 in/out
5	CH 5 IN/OUT	I/O	Channel 5 in/out
6	INH	I	Disables all channels. See Table 1.
7	V_{EE}	—	Negative power input
8	V_{SS}	—	Ground
9	C	I	Channel select C. See Table 1.
10	B	I	Channel select B. See Table 1.
11	A	I	Channel select A. See Table 1.
12	CH 3 IN/OUT	I/O	Channel 3 in/out
13	CH 0 IN/OUT	I/O	Channel 0 in/out
14	CH 1 IN/OUT	I/O	Channel 1 in/out
15	CH 2 IN/OUT	I/O	Channel 2 in/out
16	V_{DD}	—	Positive power input

Pin Functions CD4052B

PIN		I/O	DESCRIPTION
NO.	NAME		
1	Y CH 0 IN/OUT	I/O	Channel Y0 in/out
2	Y CH 2 IN/OUT	I/O	Channel Y2 in/out
3	Y COM OUT/IN	I/O	Y common out/in
4	Y CH 3 IN/OUT	I/O	Channel Y3 in/out
5	Y CH 1 IN/OUT	I/O	Channel Y1 in/out
6	INH	I	Disables all channels. See Table 1.
7	V_{EE}	—	Negative power input
8	V_{SS}	—	Ground
9	B	I	Channel select B. See Table 1.
10	A	I	Channel select A. See Table 1.
11	X CH 3 IN/OUT	I/O	Channel X3 in/out
12	X CH 0 IN/OUT	I/O	Channel X0 in/out
13	X COM IN/OUT	I/O	X common out/in
14	X CH 1 IN/OUT	I/O	Channel in/out
15	X CH 2 IN/OUT	I/O	Channel in/out
16	V_{DD}	—	Positive power input

Pin Functions CD4053B

PIN		I/O	DESCRIPTION
NO.	NAME		
1	BY IN/OUT	I/O	B channel Y in/out
2	BX IN/OUT	I/O	B channel X in/out
3	CY IN/OUT	I/O	C channel Y in/out
4	CX OR CY OUT/IN	I/O	C common out/in
5	CX IN/OUT	I/O	C channel X in/out
6	INH	I	Disables all channels. See Table 1.
7	V_{EE}	—	Negative power input
8	V_{SS}	—	Ground
9	C	I	Channel select C. See Table 1.
10	B	I	Channel select B. See Table 1.
11	A	I	Channel select A. See Table 1.
12	AX IN/OUT	I/O	A channel X in/out
13	AY IN/OUT	I/O	A channel Y in/out
14	AX OR AY OUT/IN	I/O	A common out/in
15	BX OR BY OUT/IN	I/O	B common out/in
16	V_{DD}	—	Positive power input

6 Specifications

6.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)(1).

			MIN	MAX	UNIT
	Supply Voltage	V+ to V-, Voltages Referenced to V_{SS} Terminal	–0.5	20	V
	DC Input Voltage		–0.5	V_{DD} + 0.5	V
	DC Input Current	Any One Input	–10	10	mA
T_{JMAX1}	Maximum junction temperature, ceramic package			175	°C
T_{JMAX2}	Maximum junction temperature, plastic package			150	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
CD4051B in PDIP, CDIP, SOIC, SOP, TSSOP Packages				
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	+3000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	+2000	
CD4053B in PDIP, CDIP, SOP and TSSOP Packages				
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	+2500	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	+1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted).

	MIN	MAX	UNIT
Temperature Range	–55	125	°C

6.4 Thermal Information

THERMAL METRIC(1)		CD405xB				UNIT
		E (PDIP)	M (SOIC)	NS (SOP)	PW (TSSOP)	
		16 PINS	16 PINS	16 PINS	16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	67	73	64	108	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

Over operating free-air temperature range, V_{SUPPLY} = ±5 V, and R_L = 100 Ω, (unless otherwise noted)(1).

PARAMETER			TEST CONDITIONS					MIN	TYP	MAX	UNIT
			V_{IS} (V)	V_{EE} (V)	V_{SS} (V)	V_{DD} (V)	TEMP				
SIGNAL INPUTS (V_{IS}) AND OUTPUTS (V_{OS})											
Quiescent Device Current, I_{DD} Max						5	–55°C			5	µA
							–40°C			5	
							25°C		0.04	5	
							85°C			150	
							125°C			150	
						10	–55°C			10	
							–40°C			10	
							25°C		0.04	10	
							85°C			300	
							125°C			300	
						15	–55°C			20	
							–40°C			20	
							25°C		0.04	20	
							85°C			600	
							125°C			600	
						20	–55°C			100	
							–40°C			100	
							25°C		0.08	100	
							85°C			3000	
							125°C			3000	
Drain to Source ON Resistance r_{ON} Max $0 \le V_{IS} \le V_{DD}$				0	0	5	–55°C			800	Ω
							–40°C			850	
							25°C		470	1050	
							85°C			1200	
							125°C			1300	
				0	0	10	–55°C			310	
							–40°C			300	
							25°C		180	400	
							85°C			520	
							125°C			550	
				0	0	15	–55°C			200	
							–40°C			210	
							25°C		125	240	
							85°C			300	
							125°C			300	
Change in ON Resistance (Between Any Two Channels), Δr_{ON}				0	0	5	25°C		15		Ω
				0	0	10			10		
				0	0	15			5		
OFF Channel Leakage Current: Any Channel OFF (Max) or ALL Channels OFF (Common OUT/IN) (Max)				0	0	18	–55°C			± 100	nA
							–40°C				
							25°C		± 0.01	± 100(2)	
							85°C			± 1000(2)	
							125°C				
ON Channel Leakage Current: Any Channel ON (Max) or ALL Channels ON (Common OUT/IN) (Max)			5 or 0	-5	0	10.5	85°C			± 300(3)	nA
			5	0	0	18	85°C			± 300(3)	
Capacitance	Input, C_{IS}			–5	–5	–5	25°C		5		pF
	Output, C_{OS}	CD4051					25°C		30		
		CD4052							18		
		CD4053							9		
	Feed through, C_{IOS}								0.2		

(1) Peak-to-Peak voltage symmetrical about (V_{DD} – V_{EE}) / 2.
(2) Determined by minimum feasible leakage measurement for automatic testing.
(3) Does not apply to Hi-Rel CD4051BF and CD4051BFA3 devices.

Electrical Characteristics (continued)

Over operating free-air temperature range, V_{SUPPLY} = ±5 V, and R_L = 100 Ω, (unless otherwise noted)(1).

PARAMETER		TEST CONDITIONS					MIN	TYP	MAX	UNIT
		V_{IS} (V)	V_{EE} (V)	V_{SS} (V)	V_{DD} (V)	TEMP				
Propagation Delay Time (Signal Input to Output)		V_{DD} 	R_L = 200 kΩ , C_L = 50 pF, t_r , t_f = 20 ns		5	25°C		30	60	ns
					10			15	30	
					15			10	20	
CONTROL (ADDRESS OR INHIBIT), V_C										
Input Low Voltage, V_{IL} , Max		V_{IL} = V_{DD} through 1 kΩ ; V_{IH} = V_{DD} through 1 kΩ	V_{EE} = V_{SS}, R_L = 1 kΩ to V_{SS}, I_{IS} < 2 µA on All OFF Channels		5	–55°C		1.5		V
						–40°C		1.5		
						25°C			1.5	
						85°C		1.5		
						125°C		1.5		
					10	–55°C		3		
						–40°C		3		
						25°C			3	
						85°C		3		
						125°C		3		
					15	–55°C		4		
						–40°C		4		
						25°C			4	
						85°C		4		
						125°C		4		
Input High Voltage, V_{IH} , Min					5	–55°C		3.5		V
						–40°C		3.5		
						25°C	3.5			
						85°C		3.5		
						125°C		3.5		
					10	–55°C		7		
						–40°C		7		
						25°C	7			
						85°C		7		
						125°C		7		
					15	–55°C		11		
						–40°C		11		
						25°C	11			
						85°C		11		
						125°C		11		
Input Current, I_{IN} (Max)		V_{IN} = 0, 18			18	–55°C		± 0.1		µA
						–40°C		± 0.1		
						25°C		± 10^{-5}	± 0.1	
						85°C		± 1		
						125°C		± 1		
Propagation Delay Time	Address-to-Signal OUT (Channels ON or OFF) (See Figure 10, Figure 11, and Figure 15)	t_r , t_f = 20 ns, C_L = 50 pF, R_L = 10 kΩ	0	0	5			450	720	ns
			0	0	10			160	320	
			0	0	15			120	240	
			–5	0	5			225	450	
Propagation Delay Time	Inhibit-to-Signal OUT (Channel Turning ON) (See Figure 11)	t_r , t_f = 20 ns, C_L = 50 pF, R_L = 1 kΩ	0	0	5			400	720	ns
			0	0	10			160	320	
			0	0	15			120	240	
			–10	0	5			200	400	
Propagation Delay Time	Inhibit-to-Signal OUT (Channel Turning OFF) (See Figure 17)	t_r , t_f = 20 ns, C_L = 50 pF, R_L = 10 kΩ	0	0	5			200	450	ns
			0	0	10			90	210	
			0	0	15			70	160	
			–10	0	5			130	300	
Input Capacitance, C_{IN} (Any Address or Inhibit Input)								5	7.5	pF

6.6 AC Performance Characteristics

PARAMETER	TEST CONDITIONS					TYP	UNIT
	V_{IS} (V)	V_{DD} (V)	R_L (kΩ)				
Cutoff (–3dB) Frequency Channel ON (Sine Wave Input)	5(1)	10	1	V_{OS} at Common OUT/IN	CD4053	30	MHz
					CD4052	25	
					CD4051	20	
	$V_{EE} = V_{SS}$, $20Log\frac{V_{OS}}{V_{IS}} = -3\,dB$			V_{OS} at Any Channel		60	
Total Harmonic Distortion, THD	2(1)	5	10			0.3%	
	3(1)	10				0.2%	
	5(1)	15				0.12%	
	$V_{EE} = V_{SS}$, f_{IS} = 1 kHz Sine Wave						
–40dB Feedthrough Frequency (All Channels OFF)	5(1)	10	1	V_{OS} at Common OUT/IN	CD4053	8	MHz
	$V_{EE} = V_{SS}$, $20Log\frac{V_{OS}}{V_{IS}} = -40dB$				CD4052	10	
					CD4051	12	
				V_{OS} at Any Channel		8	
–40dB Signal Crosstalk Frequency	5(1)	10	1	Between Any two Channels		3	MHz
	$V_{EE} = V_{SS}$, $20Log\frac{V_{OS}}{V_{IS}} = -40dB$			Between Sections, CD4052 Only	Measured on Common	6	
					Measured on Any Channel	10	
				Between Any Two Sections, CD4053 Only	In Pin 2, Out Pin 14	2.5	
					In Pin 15, Out Pin 14	6	
Address-or-Inhibit-to-Signal Crosstalk		10	10(2)			65	mV_{PEAK}
	V_{EE} = 0, V_{SS} = 0, t_r , t_f = 20 ns, $V_{CC} = V_{DD} – V_{SS}$ (Square Wave)					65	

(1) Peak-to-Peak voltage symmetrical about (V_{DD} - V_{EE}) / 2.
(2) Both ends of channel.

6.7 Typical Characteristics

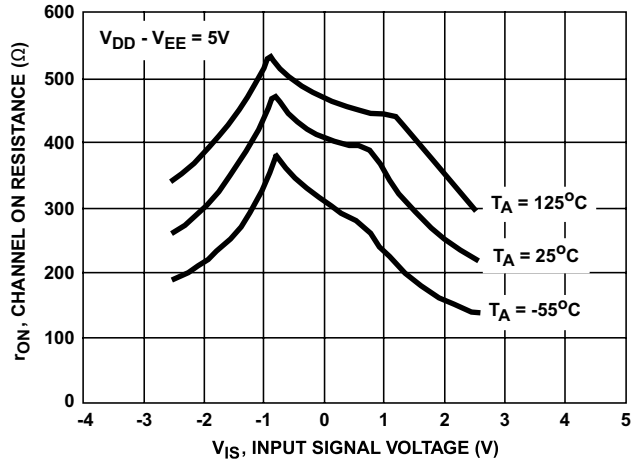


Figure 1. Channel ON Resistance vs Input Signal Voltage (All Types)

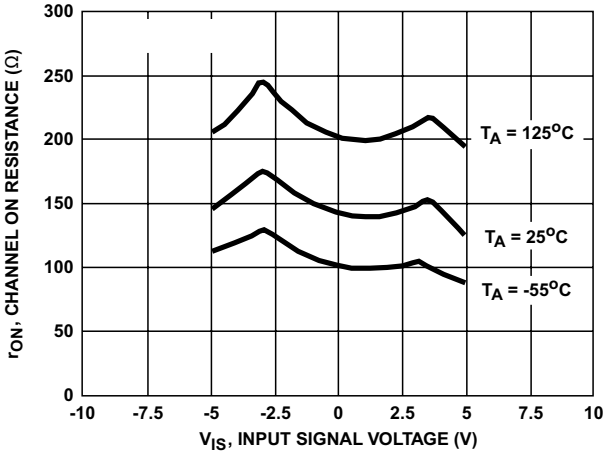


Figure 2. Channel ON Resistance vs Input Signal Voltage (All Types)

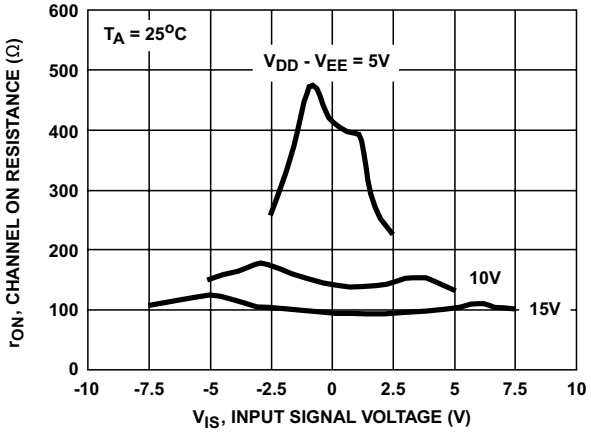


Figure 3. Channel ON Resistance vs Input Signal Voltage (All Types)

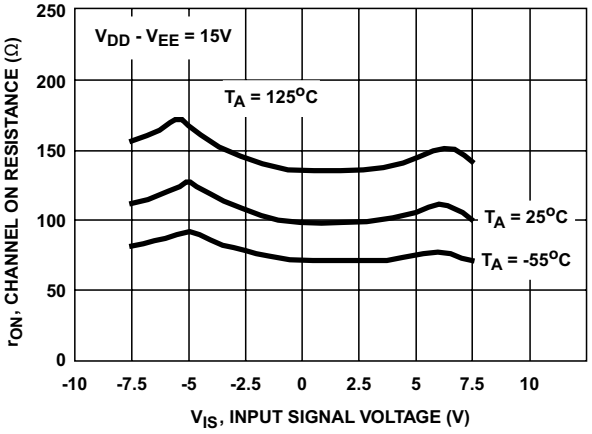


Figure 4. Channel ON Resistance vs Input Signal Voltage (All Types)

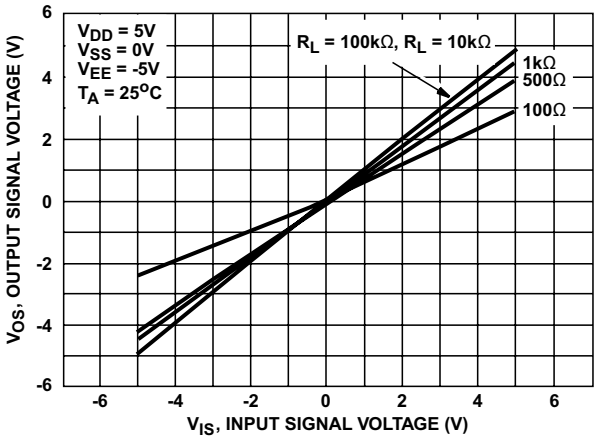


Figure 5. ON Characteristics for 1 of 8 Channels (CD4051B)

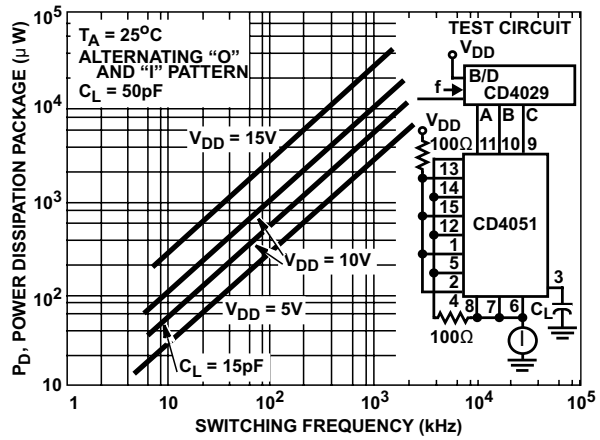


Figure 6. Dynamic Power Dissipation vs Switching Frequency (CD4051B)

Typical Characteristics (continued)

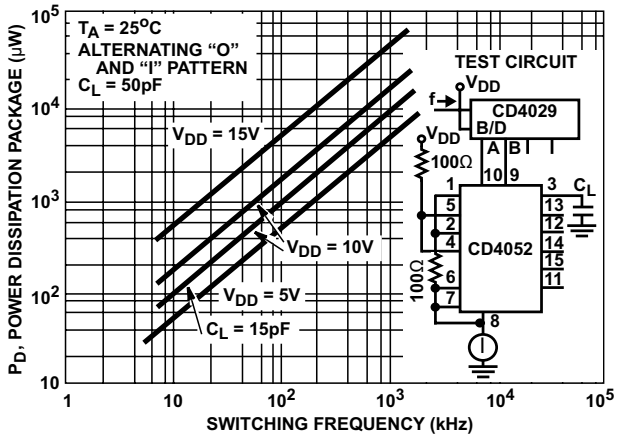


Figure 7. Dynamic Power Dissipation vs Switching Frequency (CD4052B)

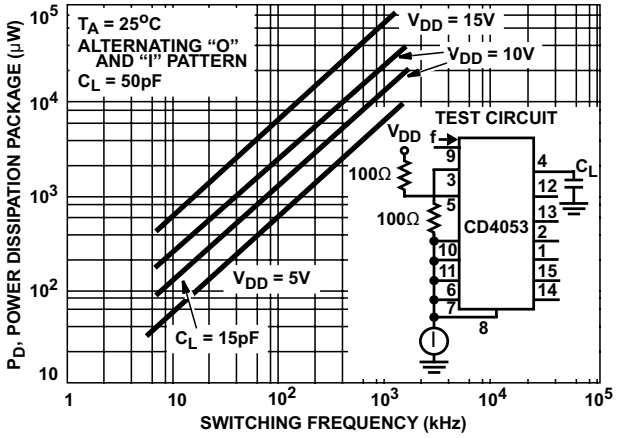


Figure 8. Dynamic Power Dissipation vs Switching Frequency (CD4053B)

7 Parameter Measurement Information

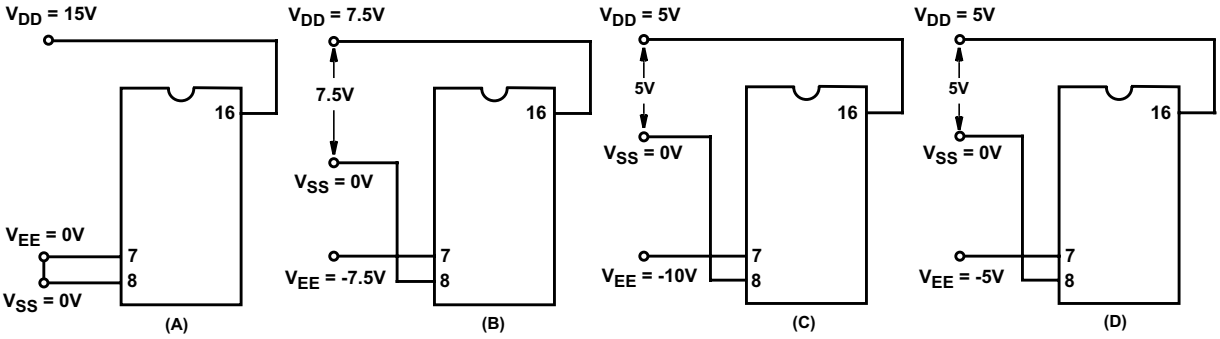


Figure 9. Typical Bias Voltages

NOTE

The ADDRESS (digital-control inputs) and INHIBIT logic levels are: 0 = V_{SS} and 1 = V_{DD}. The analog signal (through the TG) may swing from V_{EE} to V_{DD}.

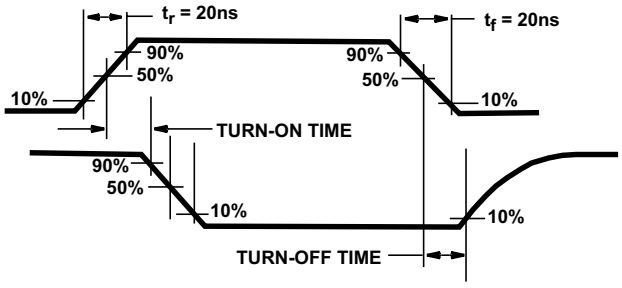


Figure 10. Waveforms, Channel Being Turned ON (R_L = 1 kΩ)

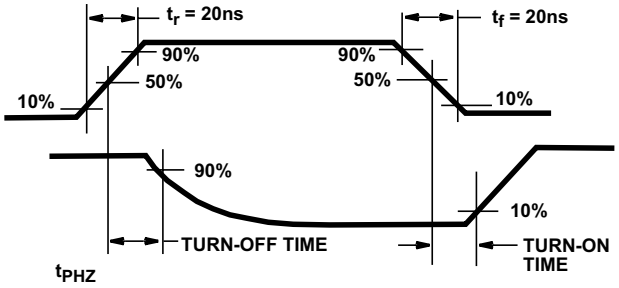


Figure 11. Waveforms, Channel Being Turned OFF (R_L = 1 kΩ)

Parameter Measurement Information (continued)

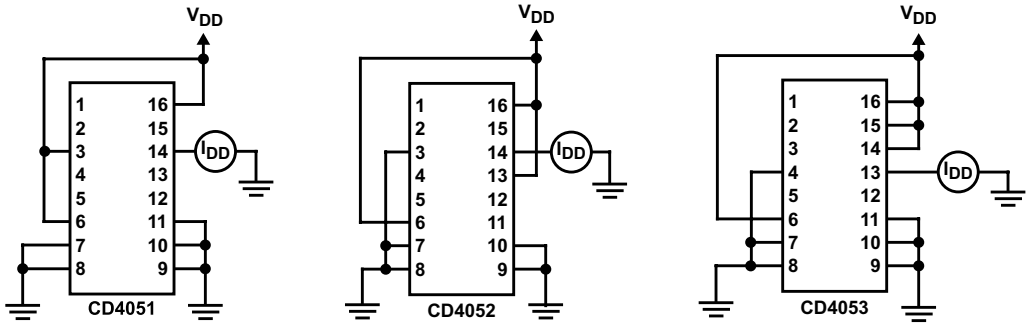


Figure 12. OFF Channel Leakage Current - Any Channel OFF

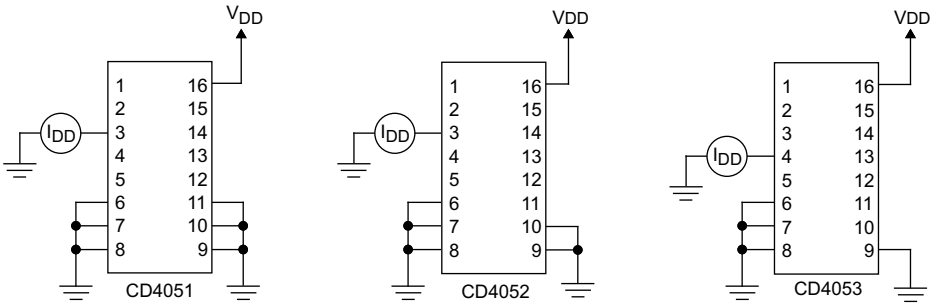


Figure 13. On Channel Leakage Current - Any Channel On

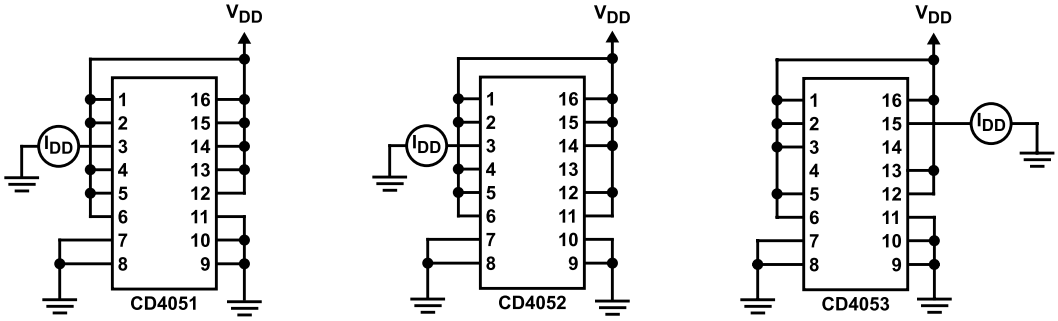


Figure 14. OFF Channel Leakage Current - All Channels OFF

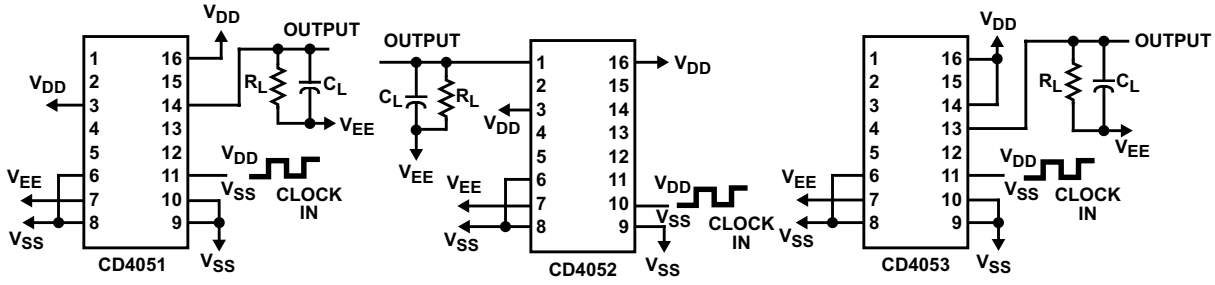


Figure 15. Propagation Delay - Address Input to Signal Output

Parameter Measurement Information (continued)

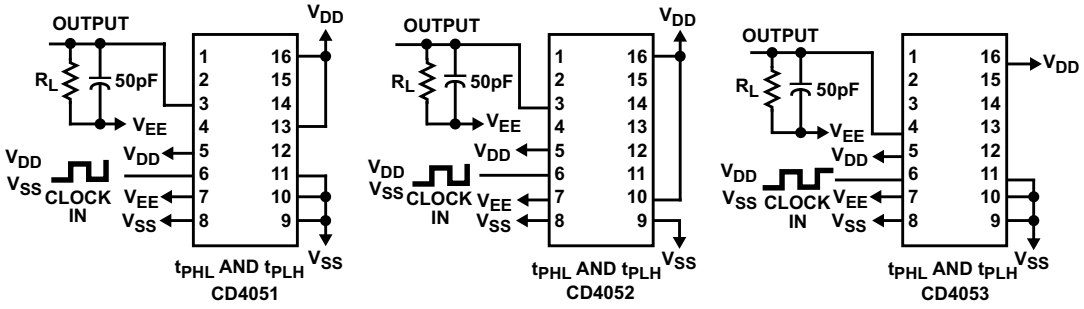


Figure 16. Propagation Delay - Inhibit Input to Signal Output

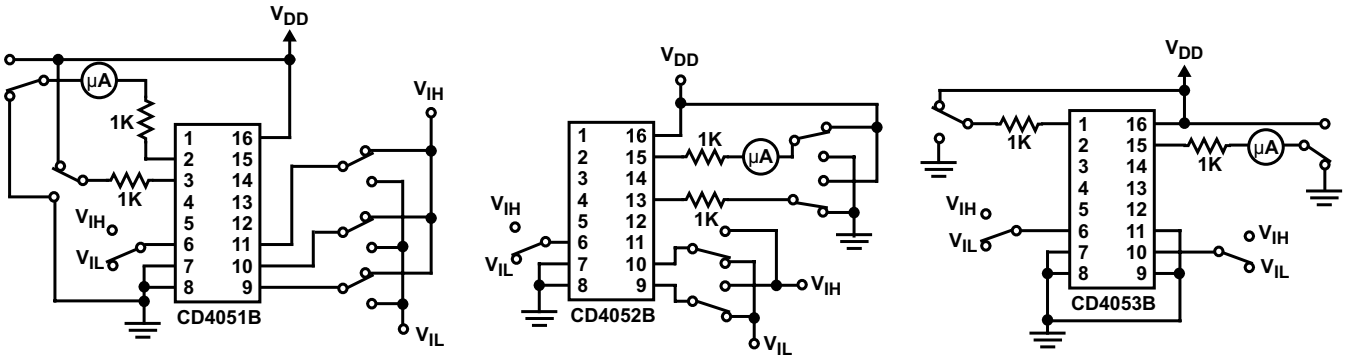


Figure 17. Input Voltage Test Circuits (Noise Immunity)

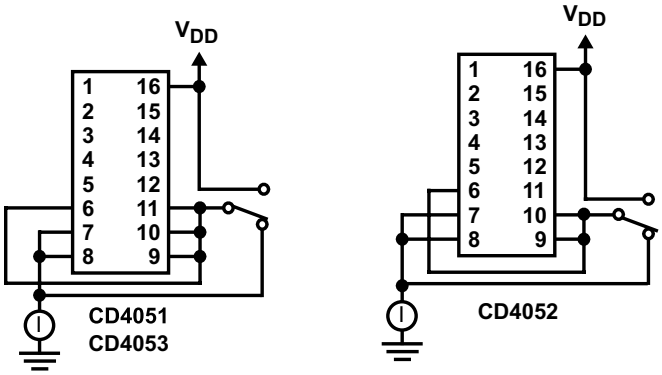


Figure 18. Quiescent Device Current

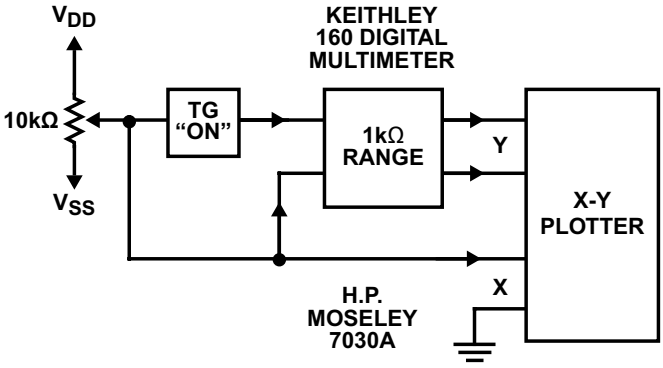
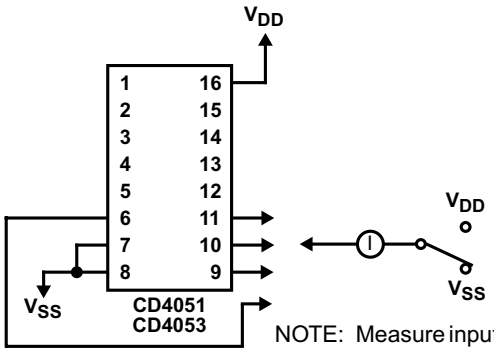
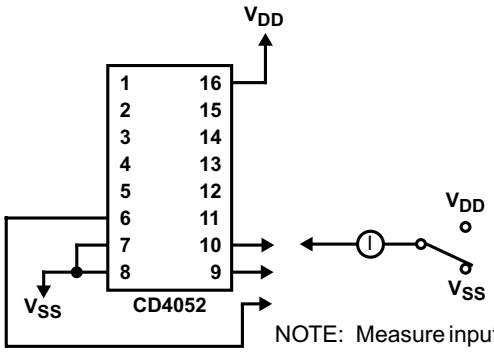


Figure 19. Channel ON Resistance Measurement Circuit

Parameter Measurement Information (continued)



NOTE: Measure inputs sequentially, to both V_{DD} and V_{SS} connect all unused inputs to either V_{DD} or V_{SS}.



NOTE: Measure inputs sequentially, to both V_{DD} and V_{SS} connect all unused inputs to either V_{DD} or V_{SS}.

Figure 20. Input Current

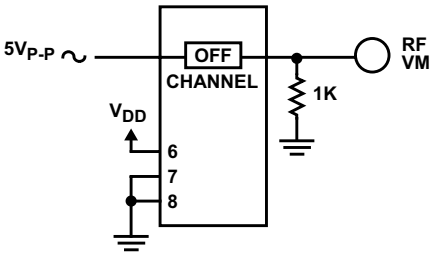


Figure 21. Feedthrough (All Types)

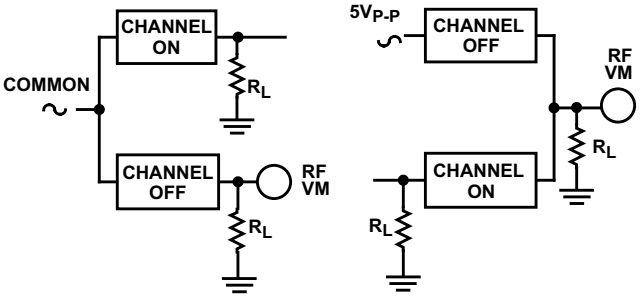
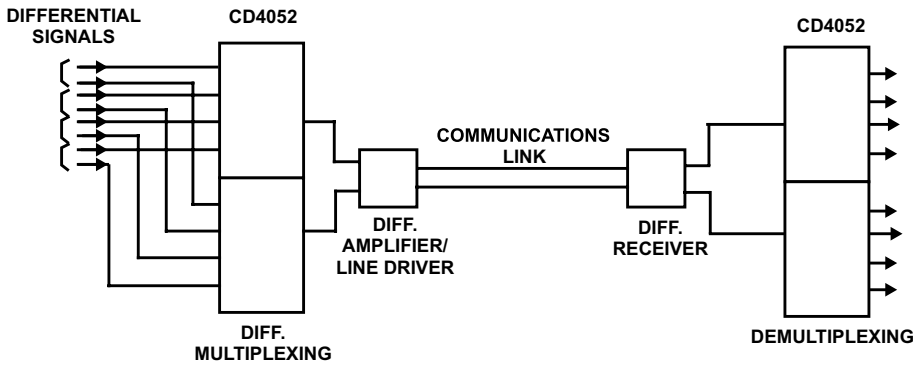


Figure 22. Crosstalk Between Any Two Channels (All Types)

Figure 23. Crosstalk Between Duals or Triplets (CD4052B, CD4053B)



Special Considerations: In applications where separate power sources are used to drive V_{DD} and the signal inputs, the V_{DD} current capability should exceed V_{DD}/R_L (R_L = effective external load). This provision avoids permanent current flow or clamp action on the V_{DD} supply when power is applied or removed from the CD4051B, CD4052B or CD4053B.

Figure 24. Typical Time-Division Application of the CD4052B

Parameter Measurement Information (continued)

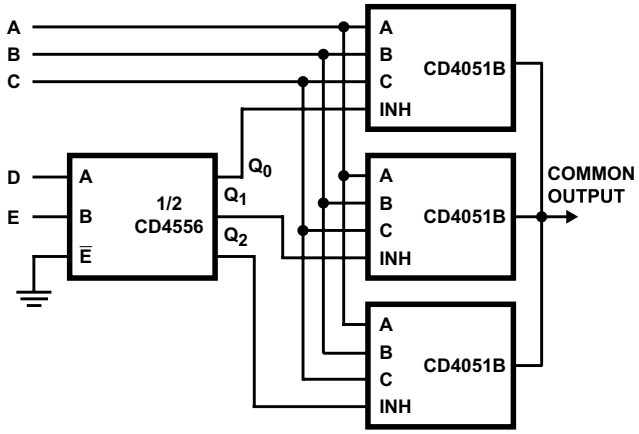


Figure 25. 24-to-1 MUX Addressing

8 Detailed Description

8.1 Overview

The CD4051B, CD4052B, and CD4053B analog multiplexers are digitally-controlled analog switches having low ON impedance and very low OFF leakage current. Control of analog signals up to 20 V_{P-P} can be achieved by digital signal amplitudes of 4.5 V to 20 V (if $V_{DD} – V_{SS}$ = 3 V, a $V_{DD} – V_{EE}$ of up to 13 V can be controlled; for $V_{DD} – V_{EE}$ level differences above 13 V, a $V_{DD} – V_{SS}$ of at least 4.5 V is required). For example, if V_{DD} = +4.5 V, V_{SS} = 0 V, and V_{EE} = –13.5 V, analog signals from –13.5 V to +4.5 V can be controlled by digital inputs of 0 V to 5 V. These multiplexer circuits dissipate extremely low quiescent power over the full $V_{DD} – V_{SS}$ and $V_{DD} – V_{EE}$ supply-voltage ranges, independent of the logic state of the control signals. When a logic 1 is present at the inhibit input terminal, all channels are off.

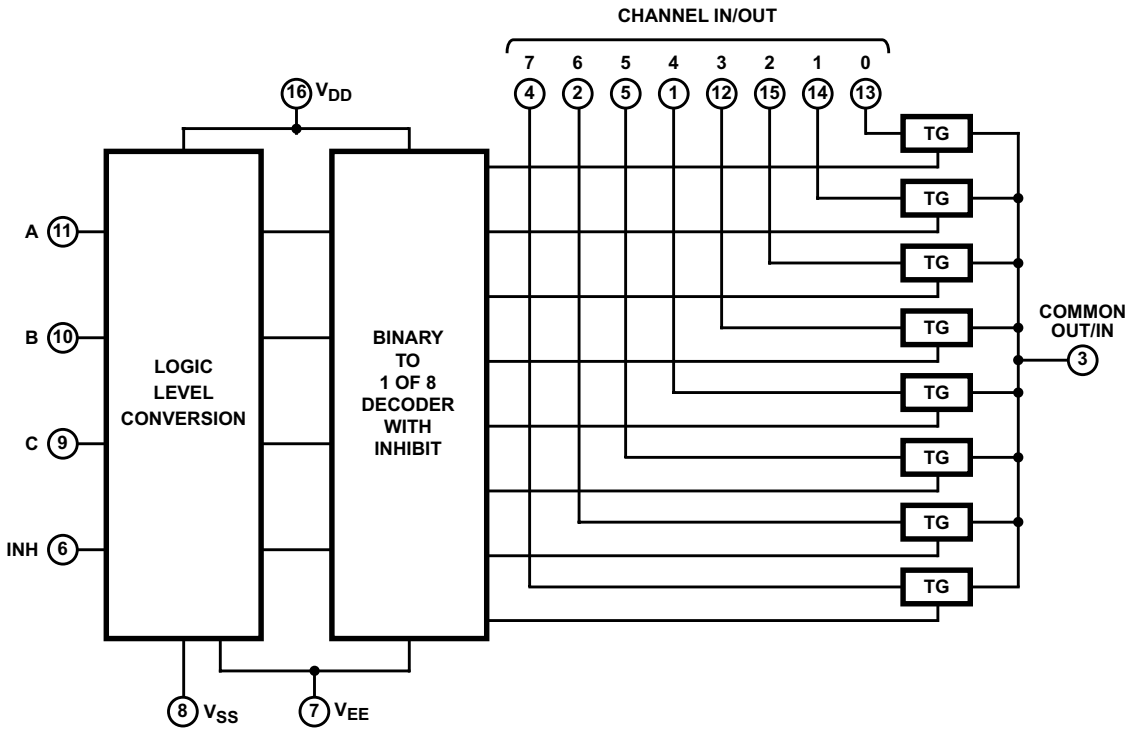
The CD4051B device is a single 8-channel multiplexer having three binary control inputs, A, B, and C, and an inhibit input. The three binary signals select 1 of 8 channels to be turned on, and connect one of the 8 inputs to the output.

The CD4052B device is a differential 4-channel multiplexer having two binary control inputs, A and B, and an inhibit input. The two binary input signals select 1 of 4 pairs of channels to be turned on and connect the analog inputs to the outputs.

The CD4053B device is a triple 2-channel multiplexer having three separate digital control inputs, A, B, and C, and an inhibit input. Each control input selects one of a pair of channels which are connected in a single-pole, double-throw configuration.

When these devices are used as demultiplexers, the CHANNEL IN/OUT terminals are the outputs and the COMMON OUT/IN terminals are the inputs.

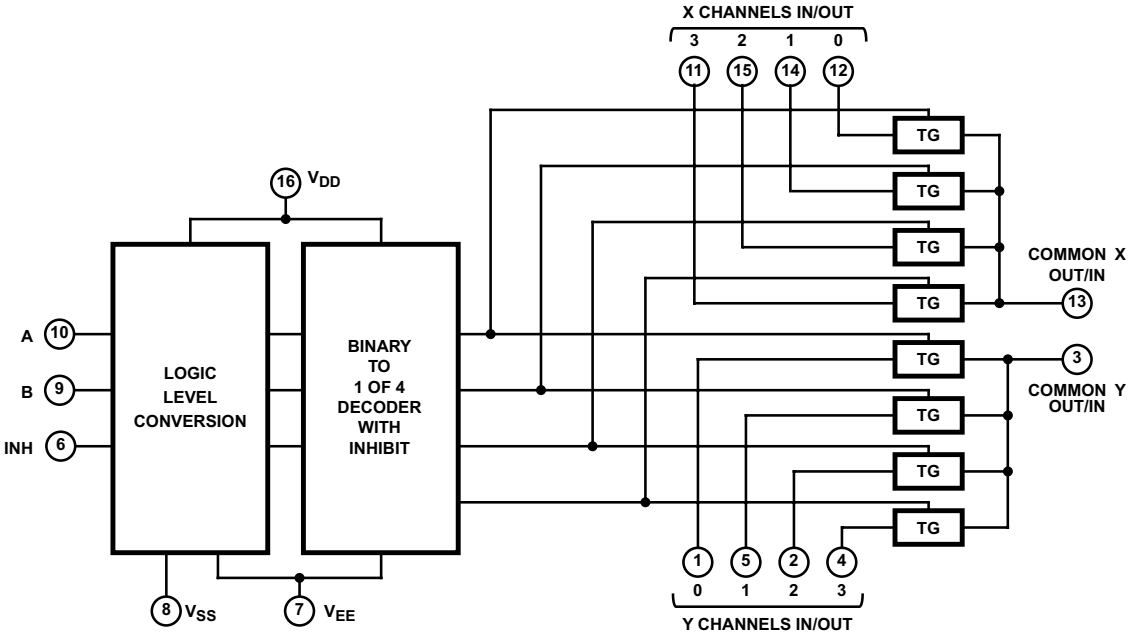
8.2 Functional Block Diagrams



All inputs are protected by standard CMOS protection network.

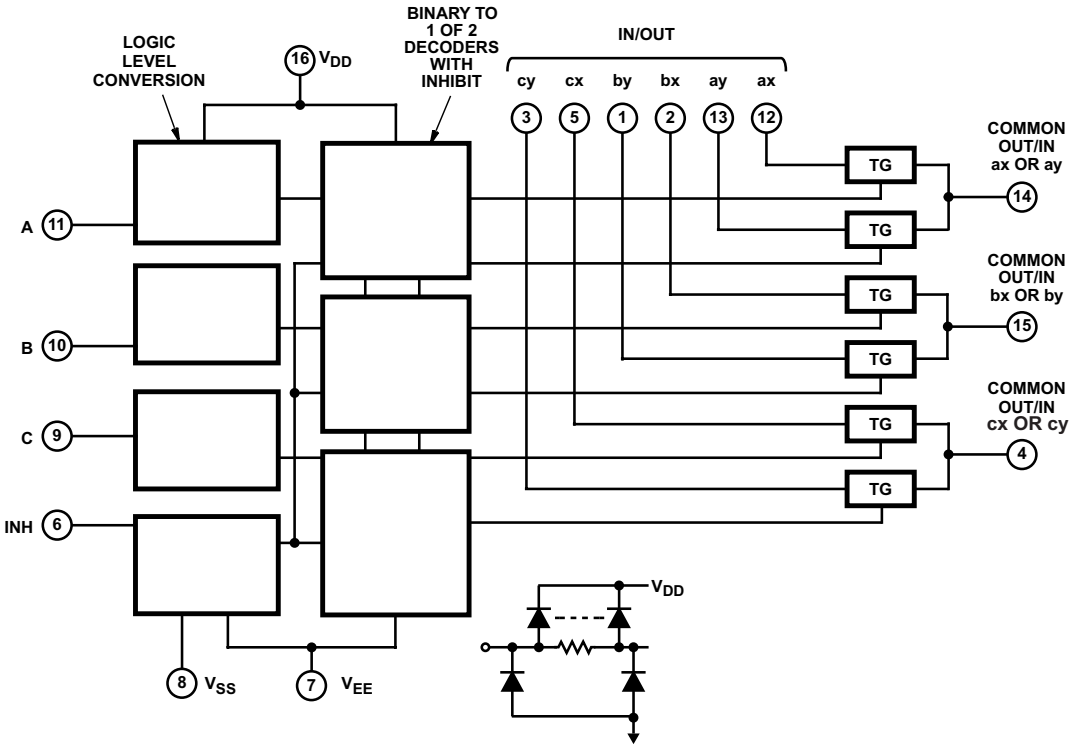
Figure 26. Functional Block Diagram, CD4051B

Functional Block Diagrams (continued)



All inputs are protected by standard CMOS protection network.

Figure 27. Functional Block Diagram, CD4052B



All inputs are protected by standard CMOS protection network.

Figure 28. Functional Block Diagram, CD4053B

8.3 Feature Description

The CD405xB line of multiplexers and demultiplexers can accept a wide range of digital and analog signal levels. Digital signals range from 3 V to 20 V, and analog signals are accepted at levels ≤ 20 V. They have low ON resistance, typically 125 Ω over 15 V_{P-P} signal input range for $V_{DD} – V_{EE}$ = 18 V. This allows for very little signal loss through the switch. Matched switch characteristics are typically r_{ON} = 5 Ω for $V_{DD} – V_{EE}$ = 15 V.

The CD405xB devices also have high OFF resistance, which keeps from wasting power when the switch is in the OFF position, with typical channel leakage of ±100 pA at $V_{DD} – V_{EE}$ = 18 V. Very low quiescent power dissipation under all digital-control input and supply conditions, typically 0.2 µW at $V_{DD} – V_{SS} = V_{DD} – V_{EE}$ = 10 V keeps power consumption total very low. All devices have been 100% tested for quiescent current at 20 V with maximum input current of 1 µA at 18 V over the full package temperature range, and only 100 nA at 18 V and 25°C.

Logic-level conversion for digital addressing signals of 3 V to 20 V ($V_{DD} – V_{SS}$ = 3 V to 20 V) to switch analog signals to 20 V_{P-P} ($V_{DD} – V_{EE}$ = 20 V). Binary address decoding on chip makes channel selection easy. When channels are changed, a break-before-make system eliminates channel overlap.

8.4 Device Functional Modes

Table 1. Truth Table(1)

INPUT STATES				ON CHANNEL(S)
INHIBIT	C	B	A	
CD4051B				
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	X	X	X	None
CD4052B				
0		0	0	0x, 0y
0		0	1	1x, 1y
0		1	0	2x, 2y
0		1	1	3x, 3y
1		X	X	None
CD4053B				
0	X	X	0	ax
0	X	X	1	ay
0	X	0	X	bx
0	X	1	X	by
0	0	X	X	cx
0	1	X	X	cy
1	X	X	X	None

(1) X = Don't Care

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The CD405xB multiplexers and demultiplexers can be used for a wide variety of applications.

9.2 Typical Application

One application of the CD4051B is to use it in conjunction with a microcontroller to poll a keypad. Figure 29 shows the basic schematic for such a polling system. The microcontroller uses the channel select pins to cycle through the different channels while reading the input to see if a user is pressing any of the keys. This is a very robust setup, allowing for multiple simultaneous key-presses with very little power consumption. It also uses very few pins on the microcontroller. The down side of polling is that the microcontroller must continually scan the keys for a press and can do little else during this process.

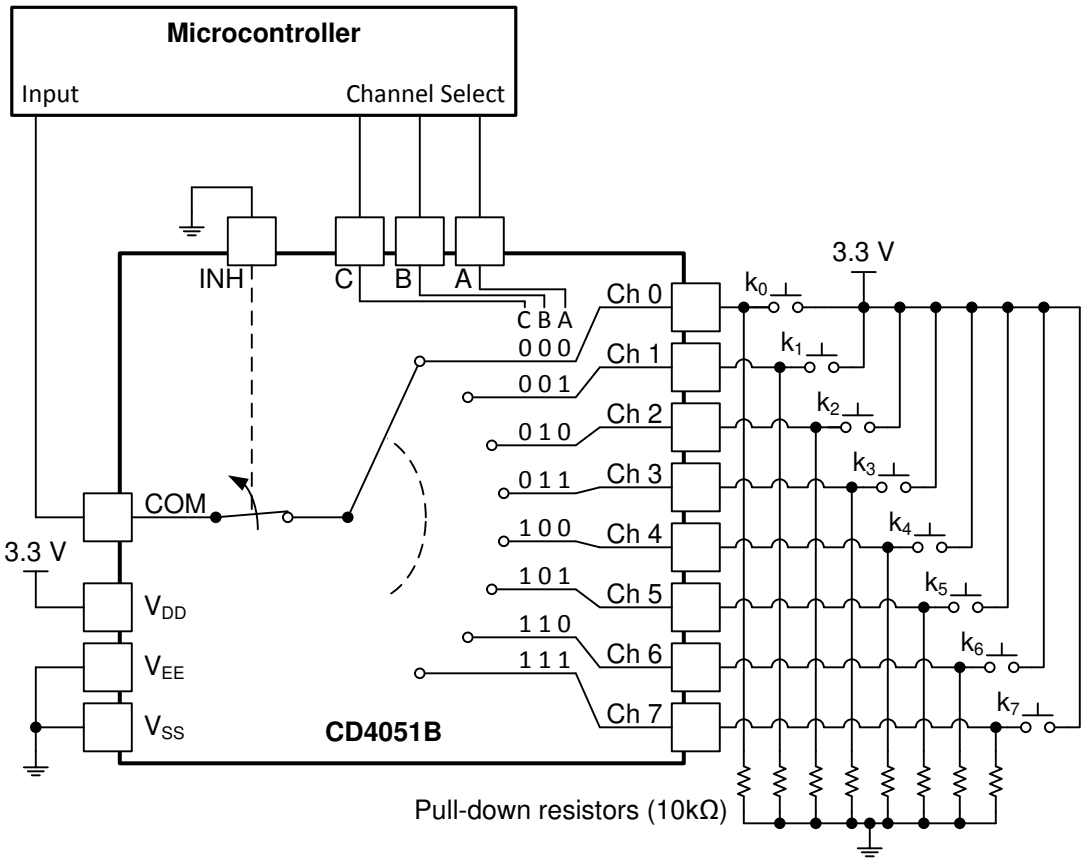


Figure 29. The CD4051B Being Used to Help Read Button Presses on a Keypad.

9.2.1 Design Requirements

These devices use CMOS technology and have balanced output drive. Take care to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive will also create fast edges into light loads, so routing and load conditions should be considered to prevent ringing.

Typical Application (continued)

9.2.2 Detailed Design Procedure

1. Recommended Input Conditions
   - For switch time specifications, see propagation delay times in *Electrical Characteristics*.
   - Inputs should not be pushed more than 0.5 V above V_{DD} or below V_{EE}.
   - For input voltage level specifications for control inputs, see V_{IH} and V_{IL} in *Electrical Characteristics*.
2. Recommended Output Conditions
   - Outputs should not be pulled above V_{DD} or below V_{EE}.
3. Input/output current consideration: The CD405xB series of parts do not have internal current drive circuitry and thus cannot sink or source current. Any current will be passed through the device.

9.2.3 Application Curve

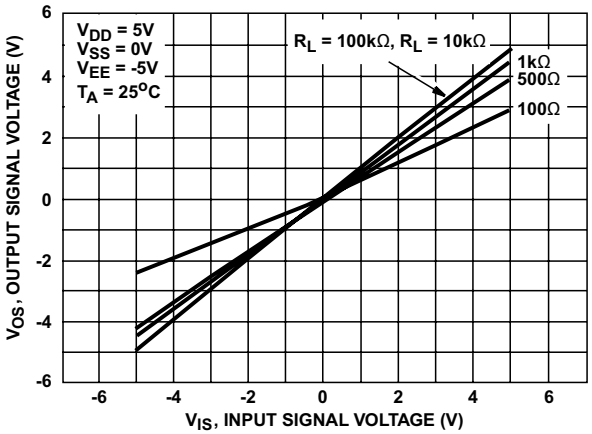


Figure 30. ON Characteristics for 1 of 8 Channels (CD4051B)

10 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Electrical Characteristics*.

Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, a 0.1-µF bypass capacitor is recommended. If there are multiple pins labeled V_{CC}, then a 0.01-µF or 0.022-µF capacitor is recommended for each V_{CC} because the V_{CC} pins will be tied together internally. For devices with dual supply pins operating at different voltages, for example V_{CC} and V_{DD}, a 0.1-µF bypass capacitor is recommended for each supply pin. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. 0.1-µF and 1-µF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

11 Layout

11.1 Layout Guidelines

Reflections and matching are closely related to loop antenna theory, but different enough to warrant their own discussion. When a PCB trace turns a corner at a 90° angle, a reflection can occur. This is primarily due to the change of width of the trace. At the apex of the turn, the trace width is increased to 1.414 times its width. This upsets the transmission line characteristics, especially the distributed capacitance and self–inductance of the trace — resulting in the reflection. It is a given that not all PCB traces can be straight, and so they will have to turn corners. Figure 31 shows progressively better techniques of rounding corners. Only the last example maintains constant trace width and minimizes reflections.

11.2 Layout Example

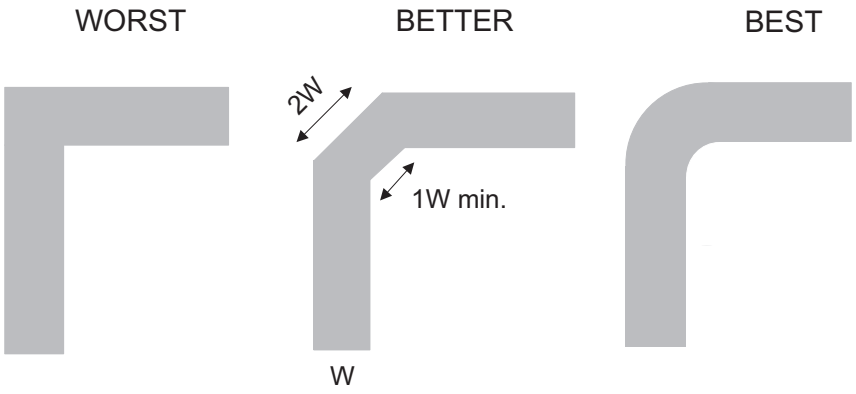


Figure 31. Trace Example

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

- *Implications of Slow or Floating CMOS Inputs*, SCBA004

12.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to order now.

Table 2. Related Links

PARTS	PRODUCT FOLDER	ORDER NOW	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
CD4051B	Click here	Click here	Click here	Click here	Click here
CD4052B	Click here	Click here	Click here	Click here	Click here
CD4053B	Click here	Click here	Click here	Click here	Click here

12.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.4 Community Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

12.5 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.6 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
7901502EA	ACTIVE	CDIP	J	16	1	Non-RoHS & Non-Green	SNPB	N / A for Pkg Type	-55 to 125	7901502EA CD4052BF3A	Samples
8101801EA	ACTIVE	CDIP	J	16	1	Non-RoHS & Non-Green	SNPB	N / A for Pkg Type	-55 to 125	8101801EA CD4053BF3A	Samples
CD4051BE	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU | SN	N / A for Pkg Type	-55 to 125	CD4051BE	Samples
CD4051BEE4	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-55 to 125	CD4051BE	Samples
CD4051BF	ACTIVE	CDIP	J	16	1	Non-RoHS & Non-Green	SNPB	N / A for Pkg Type	-55 to 125	CD4051BF	Samples
CD4051BF3A	ACTIVE	CDIP	J	16	1	Non-RoHS & Non-Green	SNPB	N / A for Pkg Type	-55 to 125	CD4051BF3A	Samples
CD4051BM	ACTIVE	SOIC	D	16	40	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4051BM	Samples
CD4051BM96	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-55 to 125	CD4051BM	Samples
CD4051BM96G3	ACTIVE	SOIC	D	16	2500	RoHS & Green	SN	Level-1-260C-UNLIM	-55 to 125	CD4051BM	Samples
CD4051BM96G4	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4051BM	Samples
CD4051BMG4	ACTIVE	SOIC	D	16	40	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4051BM	Samples
CD4051BMT	ACTIVE	SOIC	D	16	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4051BM	Samples
CD4051BNSR	ACTIVE	SO	NS	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4051B	Samples
CD4051BNSRE4	ACTIVE	SO	NS	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4051B	Samples
CD4051BPW	ACTIVE	TSSOP	PW	16	90	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM051B	Samples
CD4051BPWE4	ACTIVE	TSSOP	PW	16	90	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM051B	Samples
CD4051BPWR	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-55 to 125	CM051B	Samples
CD4051BPWRG4	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM051B	Samples
CD4052BE	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU | SN	N / A for Pkg Type	-55 to 125	CD4052BE	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CD4052BEE4	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-55 to 125	CD4052BE	Samples
CD4052BF	ACTIVE	CDIP	J	16	1	Non-RoHS & Non-Green	SNPB	N / A for Pkg Type	-55 to 125	CD4052BF	Samples
CD4052BF3A	ACTIVE	CDIP	J	16	1	Non-RoHS & Non-Green	SNPB	N / A for Pkg Type	-55 to 125	7901502EA CD4052BF3A	Samples
CD4052BM	ACTIVE	SOIC	D	16	40	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4052BM	Samples
CD4052BM96	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-55 to 125	CD4052BM	Samples
CD4052BM96E4	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4052BM	Samples
CD4052BM96G3	ACTIVE	SOIC	D	16	2500	RoHS & Green	SN	Level-1-260C-UNLIM	-55 to 125	CD4052BM	Samples
CD4052BM96G4	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4052BM	Samples
CD4052BMG4	ACTIVE	SOIC	D	16	40	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4052BM	Samples
CD4052BMT	ACTIVE	SOIC	D	16	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4052BM	Samples
CD4052BNSR	ACTIVE	SO	NS	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4052B	Samples
CD4052BPW	ACTIVE	TSSOP	PW	16	90	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM052B	Samples
CD4052BPWR	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-55 to 125	CM052B	Samples
CD4052BPWRG3	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	SN	Level-1-260C-UNLIM	-55 to 125	CM052B	Samples
CD4052BPWRG4	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM052B	Samples
CD4053BE	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-55 to 125	CD4053BE	Samples
CD4053BEE4	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-55 to 125	CD4053BE	Samples
CD4053BF	ACTIVE	CDIP	J	16	1	Non-RoHS & Non-Green	SNPB	N / A for Pkg Type	-55 to 125	CD4053BF	Samples
CD4053BF3A	ACTIVE	CDIP	J	16	1	Non-RoHS & Non-Green	SNPB	N / A for Pkg Type	-55 to 125	8101801EA CD4053BF3A	Samples
CD4053BM	ACTIVE	SOIC	D	16	40	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4053M	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CD4053BM96	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-55 to 125	CD4053M	Samples
CD4053BM96E4	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4053M	Samples
CD4053BM96G3	ACTIVE	SOIC	D	16	2500	RoHS & Green	SN	Level-1-260C-UNLIM	-55 to 125	CD4053M	Samples
CD4053BM96G4	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4053M	Samples
CD4053BMG4	ACTIVE	SOIC	D	16	40	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4053M	Samples
CD4053BMT	ACTIVE	SOIC	D	16	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4053M	Samples
CD4053BNSR	ACTIVE	SO	NS	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4053B	Samples
CD4053BPW	ACTIVE	TSSOP	PW	16	90	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM053B	Samples
CD4053BPWR	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-55 to 125	CM053B	Samples
CD4053BPWRG3	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	SN	Level-1-260C-UNLIM	-55 to 125	CM053B	Samples
CD4053BPWRG4	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM053B	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF CD4051B, CD4051B-MIL, CD4052B, CD4052B-MIL, CD4053B, CD4053B-MIL :

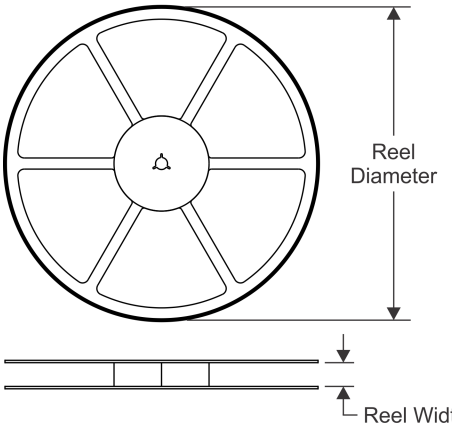
- Catalog: CD4051B, CD4052B, CD4053B
- Automotive: CD4051B-Q1, CD4051B-Q1, CD4053B-Q1, CD4053B-Q1
- Military: CD4051B-MIL, CD4052B-MIL, CD4053B-MIL

NOTE: Qualified Version Definitions:

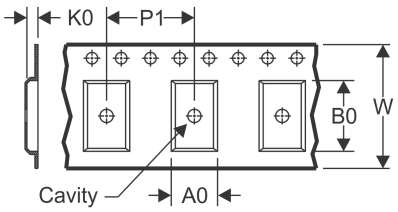
- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

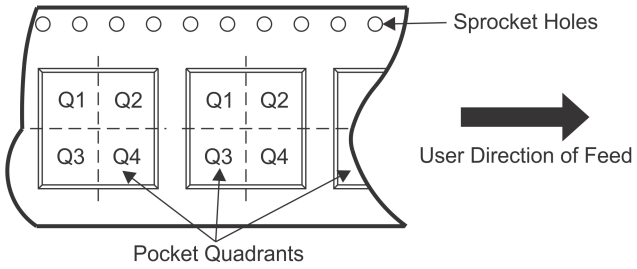


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

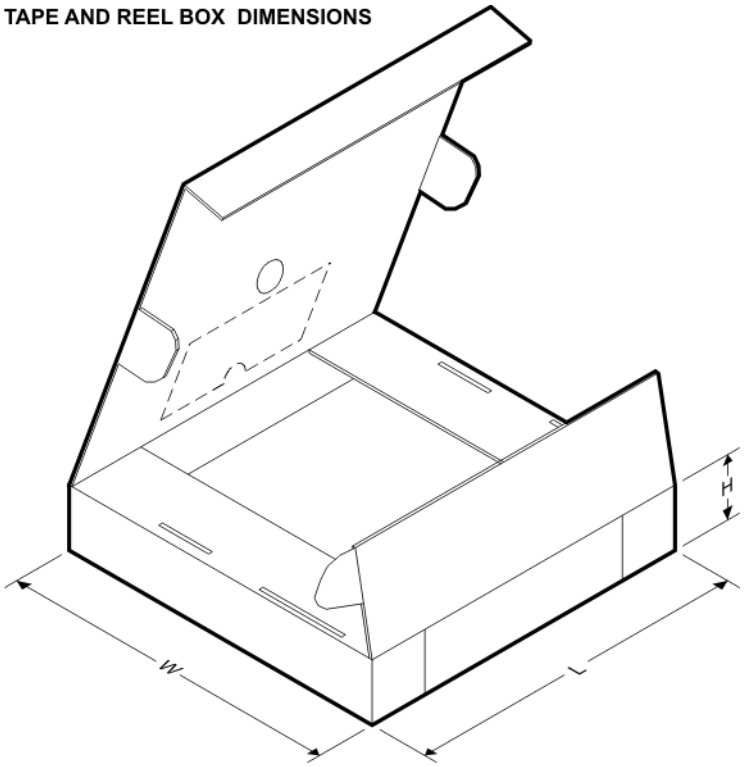


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD4051BM96	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
CD4051BM96	SOIC	D	16	2500	330.0	16.8	6.5	10.3	2.1	8.0	16.0	Q1
CD4051BM96	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
CD4051BM96G3	SOIC	D	16	2500	330.0	16.8	6.5	10.3	2.1	8.0	16.0	Q1
CD4051BM96G4	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
CD4051BM96G4	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
CD4051BNSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
CD4051BPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
CD4051BPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
CD4051BPWRG4	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
CD4052BM96	SOIC	D	16	2500	330.0	16.8	6.5	10.3	2.1	8.0	16.0	Q1
CD4052BM96	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
CD4052BM96G3	SOIC	D	16	2500	330.0	16.8	6.5	10.3	2.1	8.0	16.0	Q1
CD4052BM96G4	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
CD4052BNSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
CD4052BPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
CD4052BPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
CD4052BPWRG3	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD4052BPWRG4	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
CD4053BM96	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
CD4053BM96	SOIC	D	16	2500	330.0	16.8	6.5	10.3	2.1	8.0	16.0	Q1
CD4053BM96G3	SOIC	D	16	2500	330.0	16.8	6.5	10.3	2.1	8.0	16.0	Q1
CD4053BM96G4	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
CD4053BNSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
CD4053BPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
CD4053BPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
CD4053BPWRG3	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
CD4053BPWRG4	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

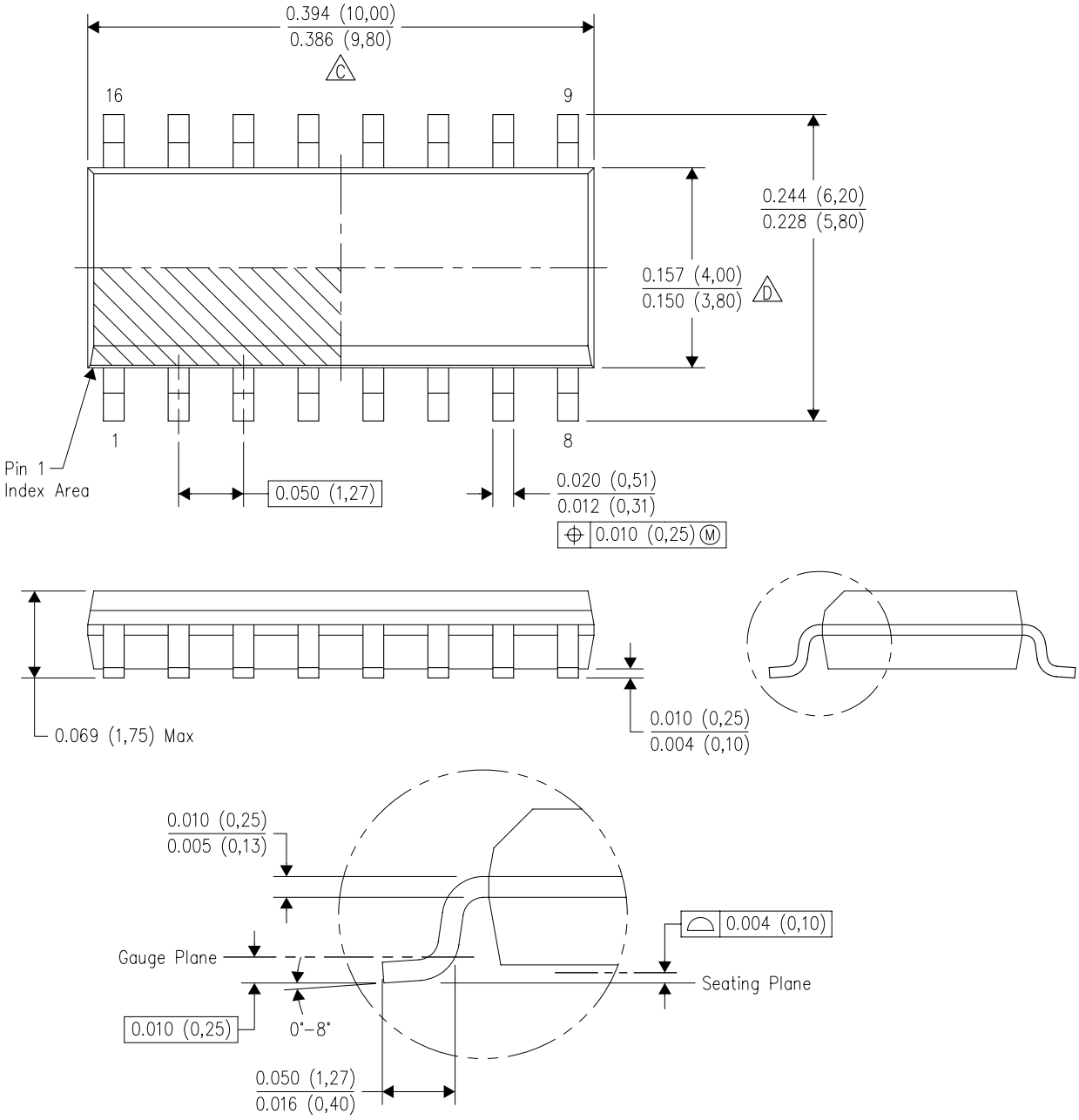


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD4051BM96	SOIC	D	16	2500	853.0	449.0	35.0
CD4051BM96	SOIC	D	16	2500	364.0	364.0	27.0
CD4051BM96	SOIC	D	16	2500	333.2	345.9	28.6
CD4051BM96G3	SOIC	D	16	2500	364.0	364.0	27.0
CD4051BM96G4	SOIC	D	16	2500	333.2	345.9	28.6
CD4051BM96G4	SOIC	D	16	2500	853.0	449.0	35.0
CD4051BNSR	SO	NS	16	2000	853.0	449.0	35.0

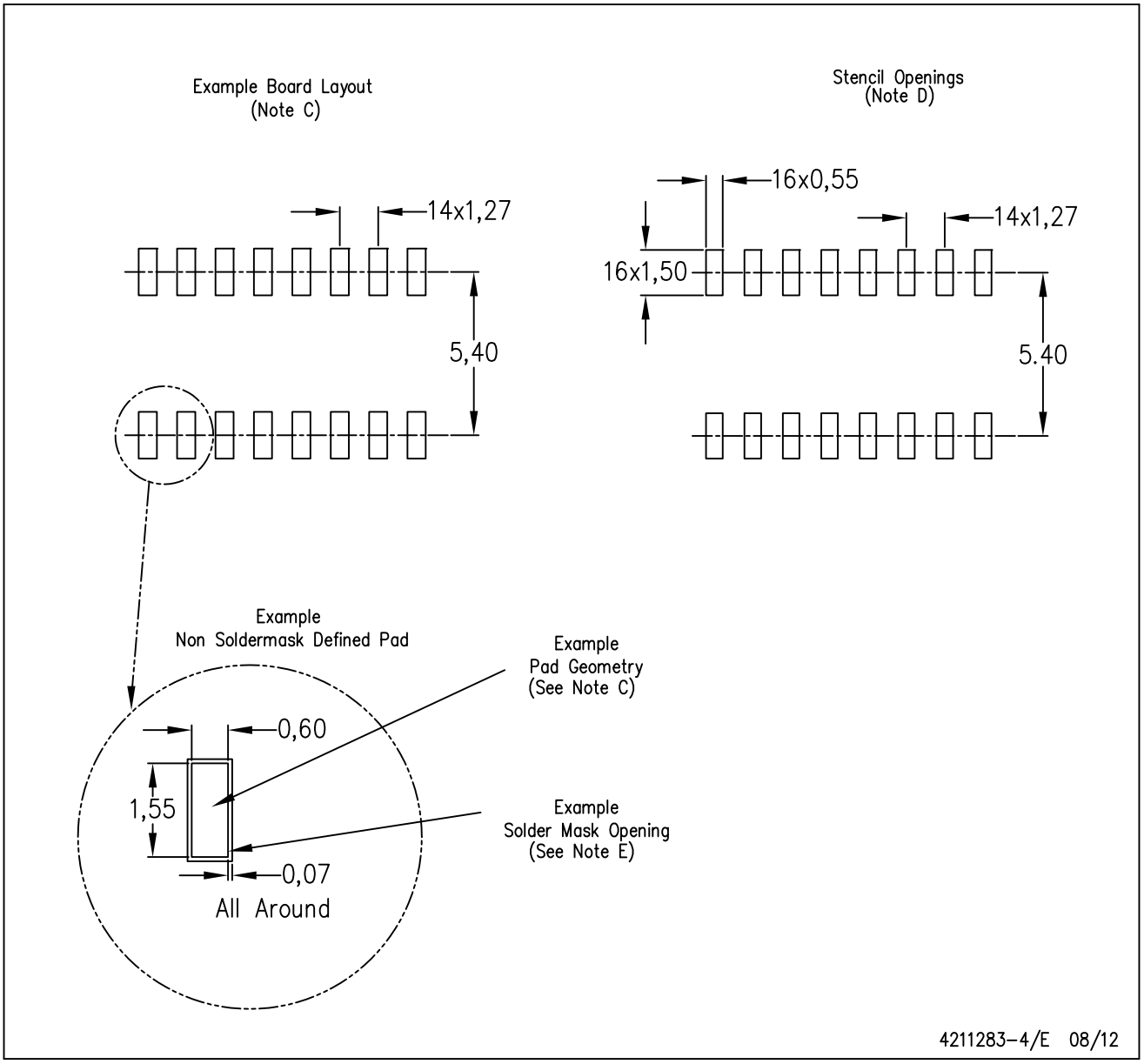
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD4051BPWR	TSSOP	PW	16	2000	364.0	364.0	27.0
CD4051BPWR	TSSOP	PW	16	2000	367.0	367.0	35.0
CD4051BPWRG4	TSSOP	PW	16	2000	367.0	367.0	35.0
CD4052BM96	SOIC	D	16	2500	364.0	364.0	27.0
CD4052BM96	SOIC	D	16	2500	333.2	345.9	28.6
CD4052BM96G3	SOIC	D	16	2500	364.0	364.0	27.0
CD4052BM96G4	SOIC	D	16	2500	333.2	345.9	28.6
CD4052BNSR	SO	NS	16	2000	853.0	449.0	35.0
CD4052BPWR	TSSOP	PW	16	2000	367.0	367.0	35.0
CD4052BPWR	TSSOP	PW	16	2000	364.0	364.0	27.0
CD4052BPWRG3	TSSOP	PW	16	2000	364.0	364.0	27.0
CD4052BPWRG4	TSSOP	PW	16	2000	367.0	367.0	35.0
CD4053BM96	SOIC	D	16	2500	333.2	345.9	28.6
CD4053BM96	SOIC	D	16	2500	364.0	364.0	27.0
CD4053BM96G3	SOIC	D	16	2500	364.0	364.0	27.0
CD4053BM96G4	SOIC	D	16	2500	333.2	345.9	28.6
CD4053BNSR	SO	NS	16	2000	853.0	449.0	35.0
CD4053BPWR	TSSOP	PW	16	2000	364.0	364.0	27.0
CD4053BPWR	TSSOP	PW	16	2000	367.0	367.0	35.0
CD4053BPWRG3	TSSOP	PW	16	2000	364.0	364.0	27.0
CD4053BPWRG4	TSSOP	PW	16	2000	367.0	367.0	35.0

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



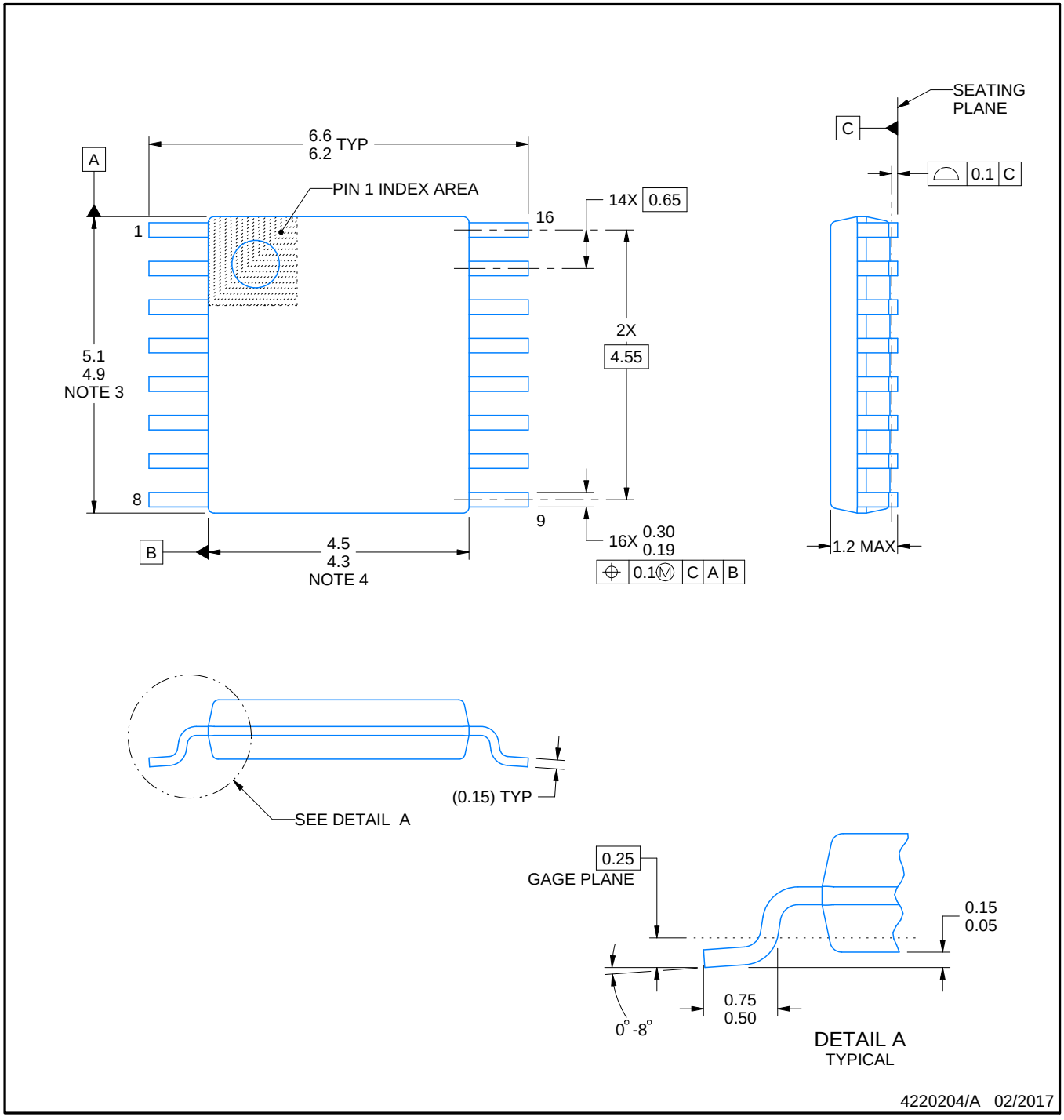
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PACKAGE OUTLINE

PW0016A

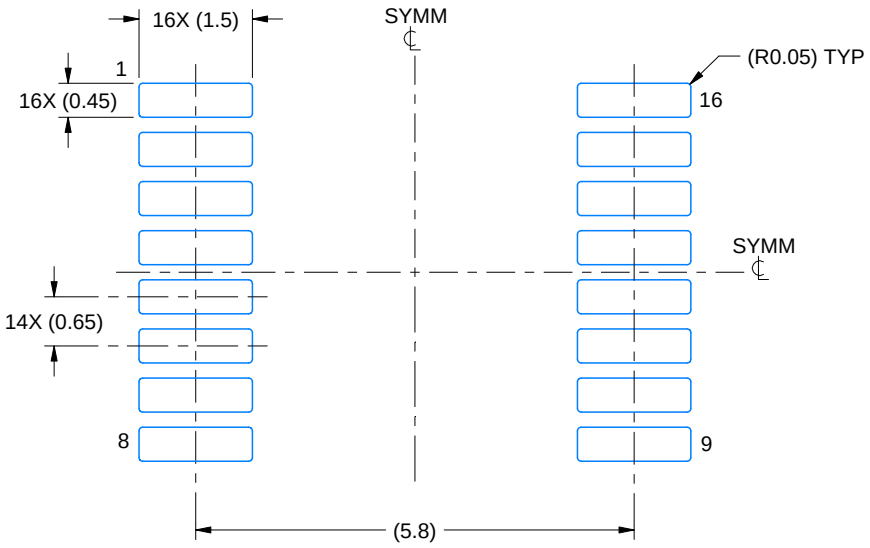
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

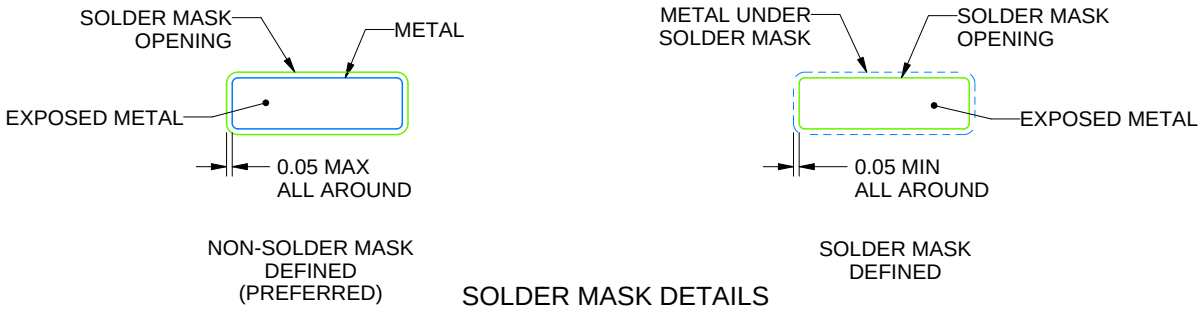


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

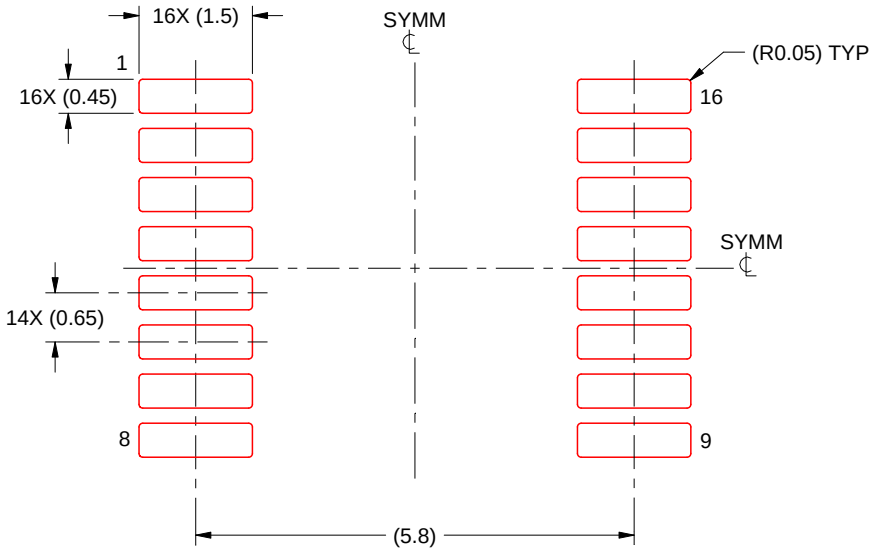


SOLDER MASK DETAILS

4220204/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/A 02/2017

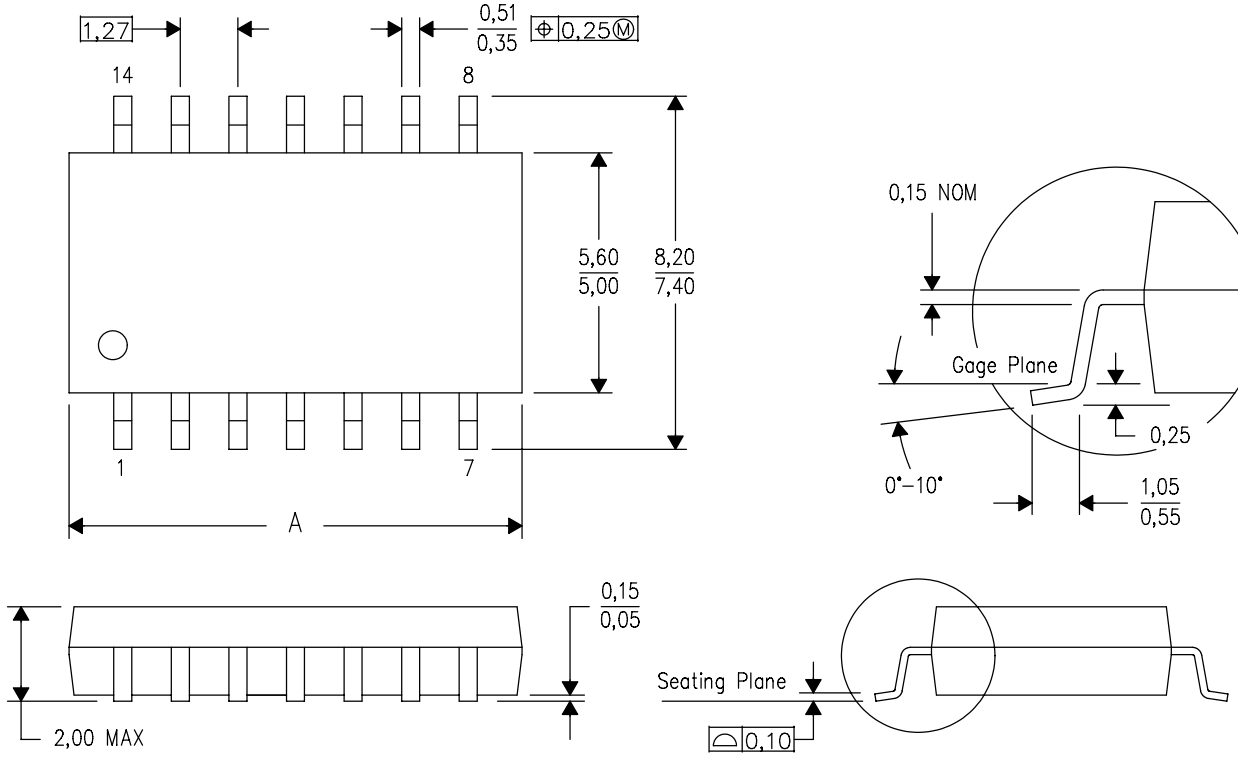
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN



DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

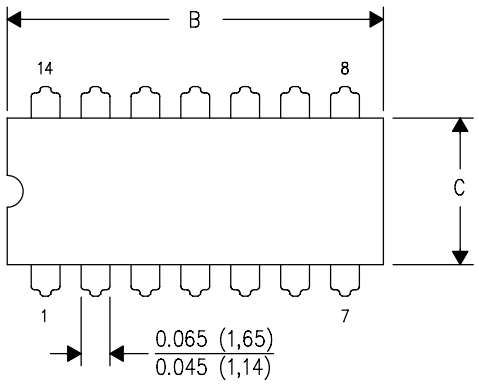
4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

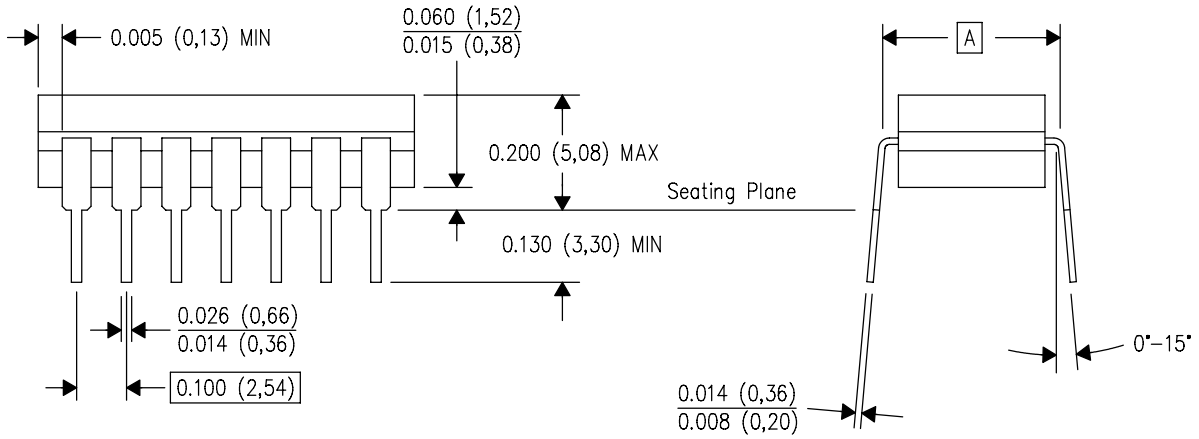
J (R–GDIP–T**)

14 LEADS SHOWN

CERAMIC DUAL IN–LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



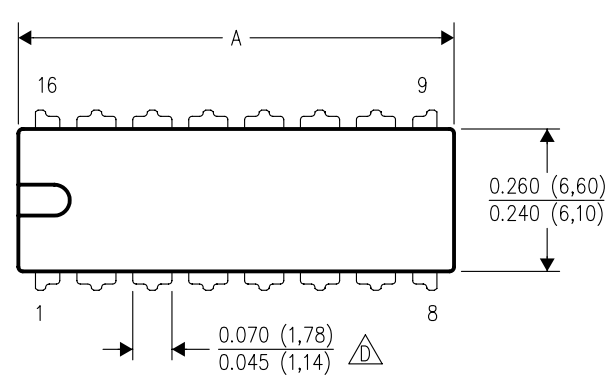
4040083/F 03/03

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

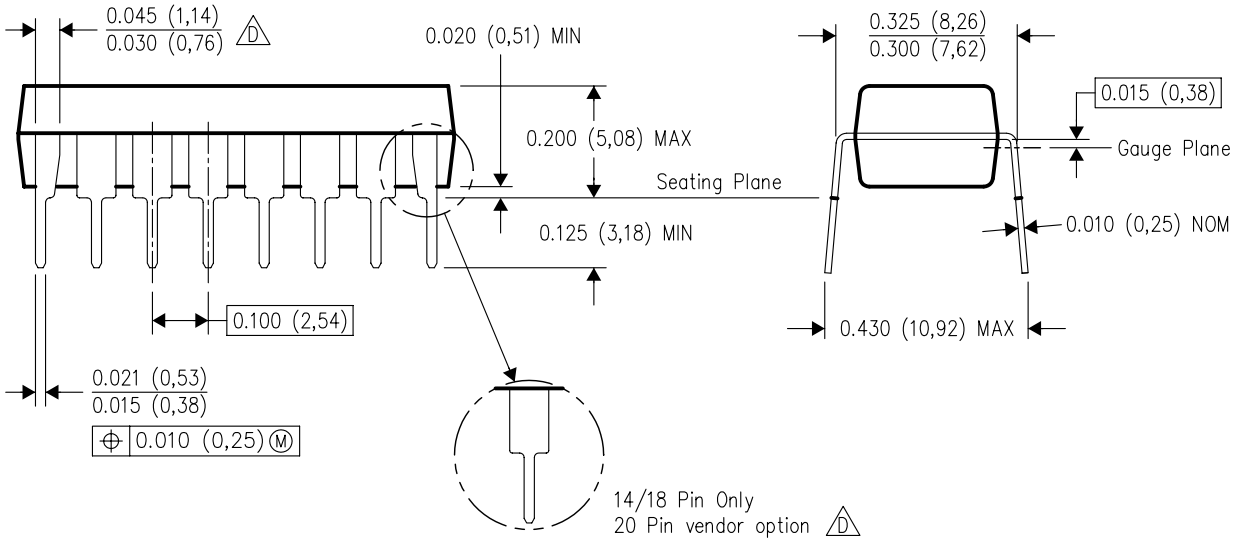
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

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