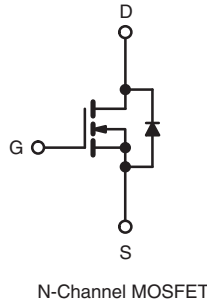
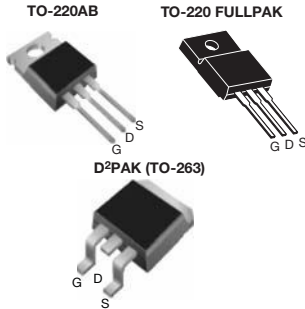




Power MOSFET

| PRODUCT SUMMARY | |
|--|-------------------------------|
| V _{DS} (V) at T _J max. | 560 |
| R _{DS(on)} (Ω) | V _{GS} = 10 V 0.38 |
| Q _g (Max.) (nC) | 68 |
| Q _{gs} (nC) | 17.6 |
| Q _{gd} (nC) | 21.8 |
| Configuration | Single |



FEATURES

- Low Figure-of-Merit R_{on} x Q_g
- 100 % Avalanche Tested
- Gate Charge Improved
- T_{rr}/Q_{rr} Improved
- Compliant to RoHS Directive 2002/95/EC



Note

* Pb containing terminations are not RoHS compliant, exemptions may apply

| ORDERING INFORMATION | | | |
|----------------------|---------------|-----------------------------|----------------|
| Package | TO-220AB | D ² PAK (TO-263) | TO-220 FULLPAK |
| | SiHP16N50C-E3 | SiHB16N50C-E3 | SiHF16N50C-E3 |
| Lead (Pb)-free | - | SiHB16N50CTR-E3 | - |
| | - | SiHB16N50CTL-E3 | - |

| ABSOLUTE MAXIMUM RATINGS (T _C = 25 °C, unless otherwise noted) | | | | |
|---|---------------------------------------|-----------------------------------|---------------|------|
| PARAMETER | | SYMBOL | LIMIT | UNIT |
| Drain-Source Voltage | | V _{DS} | 500 | V |
| Gate-Source Voltage | | V _{GS} | ± 30 | |
| Continuous Drain Current (T _J = 150 °C) ^a | V _{GS} at 10 V | T _C = 25 °C | 16 | A |
| | | T _C = 100 °C | 10 | |
| Pulsed Drain Current ^c | | I _{DM} | 40 | |
| Linear Derating Factor | | | 2 | W/°C |
| Single Pulse Avalanche Energy ^b | | E _{AS} | 320 | mJ |
| Maximum Power Dissipation | TO220-AB, D ² PAK (TO-263) | P _D | 250 | W |
| | TO-220 FULLPAK | | 38 | |
| Operating Junction and Storage Temperature Range | | T _J , T _{stg} | - 55 to + 150 | °C |
| Soldering Recommendations (Peak Temperature) ^d | | for 10 s | 300 | |

Notes


- Limited by maximum junction temperature.
- V_{DD} = 50 V, starting T_J = 25 °C, L = 2.5 mH, R_g = 25 Ω, I_{AS} = 16 A.
- Repetitive rating; pulse width limited by maximum junction temperature.
- 1.6 mm from case.



| THERMAL RESISTANCE RATINGS | | | | |
|--|-------------------|--------------------------------------|----------------|------|
| PARAMETER | SYMBOL | TO220-AB D ² PAK (TO-263) | TO-220 FULLPAK | UNIT |
| Maximum Junction-to-Ambient | R _{thJA} | 62 | 65 | °C/W |
| Maximum Junction-to-Case (Drain) | R _{thJC} | 0.5 | 3.3 | |
| Junction-to-Ambient (PCB mount) ^a | R _{thJA} | 40 | - | |

Note

a. When mounted on 1" square PCB (FR-4 or G-10 material).

| SPECIFICATIONS (T _J = 25 °C, unless otherwise noted) | | | | | | |
|---|----------------------------------|---|------|------|-------|------|
| PARAMETER | SYMBOL | TEST CONDITIONS | MIN. | TYP. | MAX. | UNIT |
| Static | | | | | | |
| Drain-Source Breakdown Voltage | V _{DS} | V _{GS} = 0 V, I _D = 250 μA | 500 | - | - | V |
| V _{DS} Temperature Coefficient | ΔV _{DS} /T _J | Reference to 25 °C, I _D = 1 mA | - | 0.6 | - | V/°C |
| Gate-Source Threshold Voltage (N) | V _{GS(th)} | V _{DS} = V _{GS} , I _D = 250 μA | 3.0 | - | 5.0 | V |
| Gate-Source Leakage | I _{GSS} | V _{GS} = ± 30 V | - | - | ± 100 | nA |
| Zero Gate Voltage Drain Current | I _{DSS} | V _{DS} = 500 V, V _{GS} = 0 V | - | - | 50 | μA |
| | | V _{DS} = 400 V, V _{GS} = 0 V, T _J = 125 °C | - | - | 250 | |
| Drain-Source On-State Resistance | R _{DS(on)} | V _{GS} = 10 V, I _D = 8 A | - | 0.31 | 0.38 | Ω |
| Forward Transconductance ^a | g _{fs} | V _{DS} = 50 V, I _D = 3 A | - | 3 | - | S |
| Dynamic | | | | | | |
| Input Capacitance | C _{iss} | V _{GS} = 0 V, V _{DS} = 25 V, f = 1.0 MHz | - | 1900 | - | pF |
| Output Capacitance | C _{oss} | | - | 230 | - | |
| Reverse Transfer Capacitance | C _{rss} | | - | 24 | - | |
| Total Gate Charge | Q _g | V _{GS} = 10 V, I _D = 16 A, V _{DS} = 400 V | - | 45 | 68 | nC |
| Gate-Source Charge | Q _{gs} | | - | 18 | - | |
| Gate-Drain Charge | Q _{gd} | | - | 22 | - | |
| Turn-On Delay Time | t _{d(on)} | V _{DD} = 250 V, I _D = 16 A, R _g = 9.1 Ω, V _{GS} = 10 V | - | 27 | - | ns |
| Rise Time | t _r | | - | 156 | - | |
| Turn-Off Delay Time | t _{d(off)} | | - | 29 | - | |
| Fall Time | t _f | | - | 31 | - | |
| Gate Input Resistance | R _g | f = 1 MHz, open drain | - | 1.6 | - | Ω |
| Drain-Source Body Diode Characteristics | | | | | | |
| Continuous Source-Drain Diode Current | I _S | MOSFET symbol showing the integral reverse p - n junction diode  | - | - | 16 | A |
| Pulsed Diode Forward Current | I _{SM} | | - | - | 30 | |
| Body Diode Voltage | V _{SD} | T _J = 25 °C, I _S = 10 A, V _{GS} = 0 V | - | - | 1.8 | V |
| Body Diode Reverse Recovery Time | t _{rr} | T _J = 25 °C, I _F = I _S , dI/dt = 100 A/μs, V _R = 20 V | - | 555 | - | ns |
| Body Diode Reverse Recovery Charge | Q _{rr} | | - | 5.5 | - | μC |
| Body Diode Reverse Recovery Current | I _{RRM} | | - | 18 | - | A |

Note

- The information shown here is a preliminary product proposal, not a commercial product data sheet. Vishay Siliconix is not committed to produce this or any similar product. This information should not be used for design purposes, nor construed as an offer to furnish or sell such products.



TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

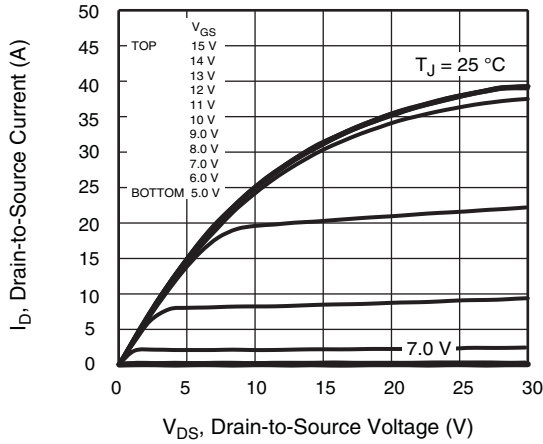


Fig. 1 - Typical Output Characteristics (TO-220)

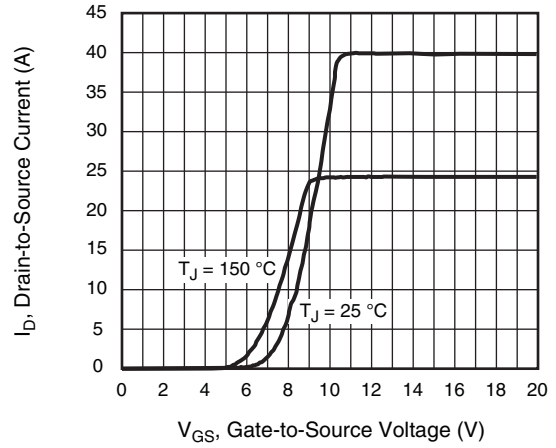


Fig. 3 - Typical Transfer Characteristics

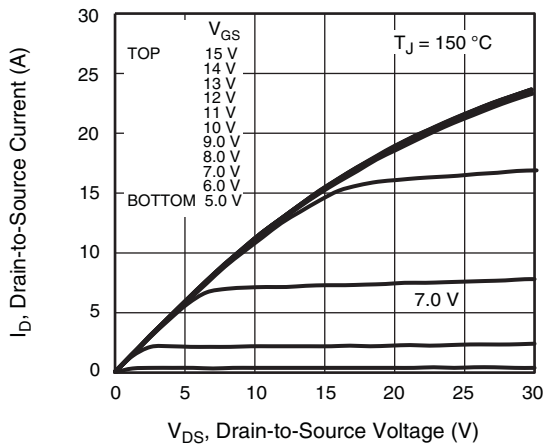


Fig. 2 - Typical Output Characteristics (TO-220)

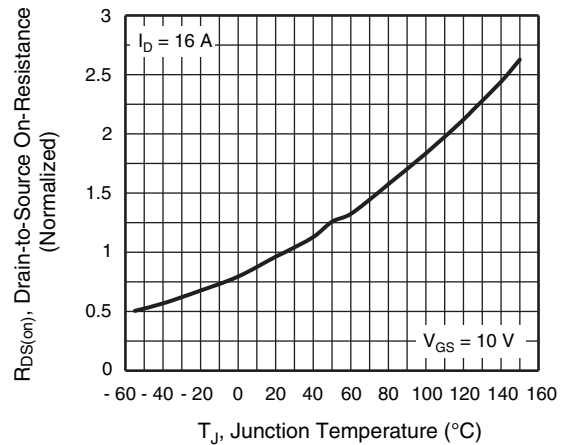


Fig. 4 - Normalized On-Resistance vs. Temperature

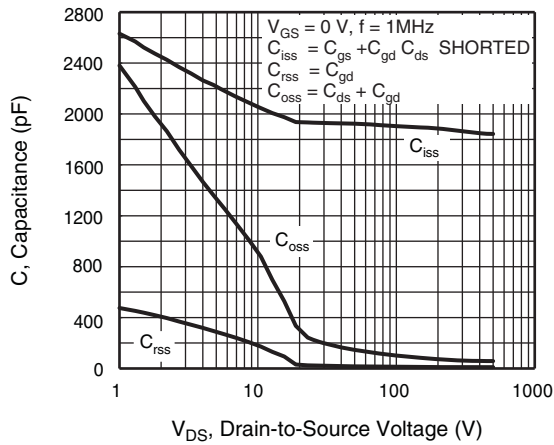


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

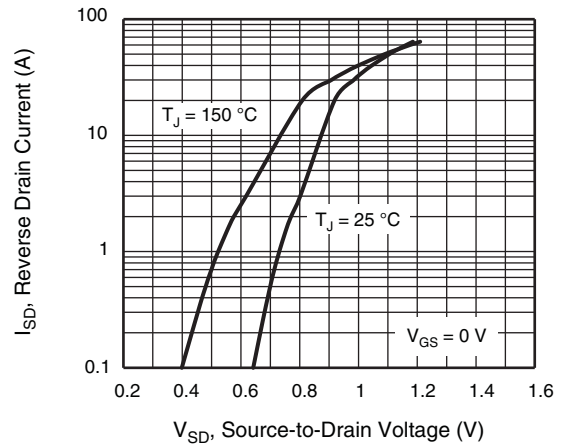


Fig. 7 - Typical Source-Drain Diode Forward Voltage

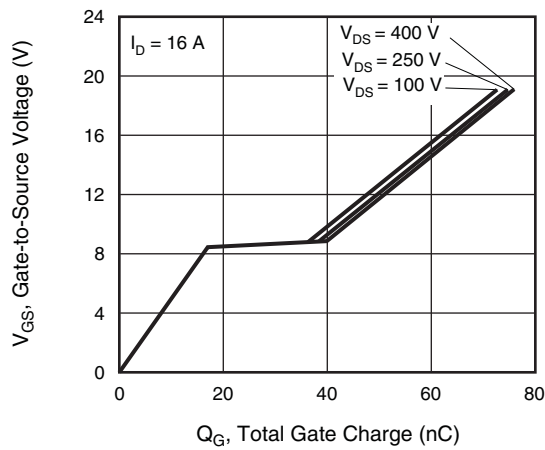


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

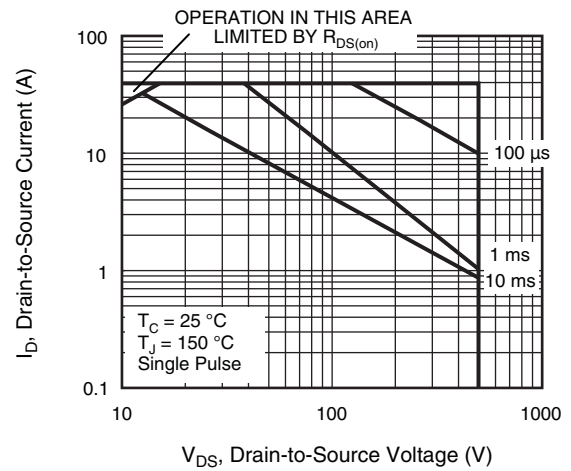


Fig. 8 - Maximum Safe Operating Area (TO-220AB, D²PAK)

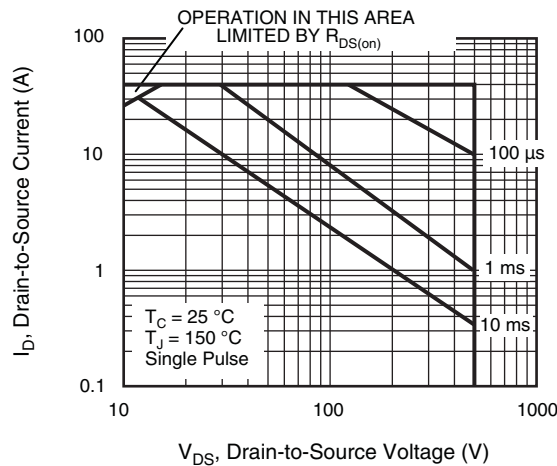


Fig. 9 - Maximum Safe Operating Area (TO-220 FULLPAK)

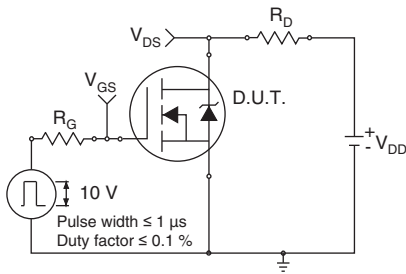


Fig. 10a - Switching Time Test Circuit

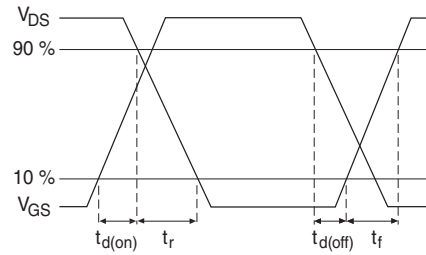


Fig. 10b - Switching Time Waveforms

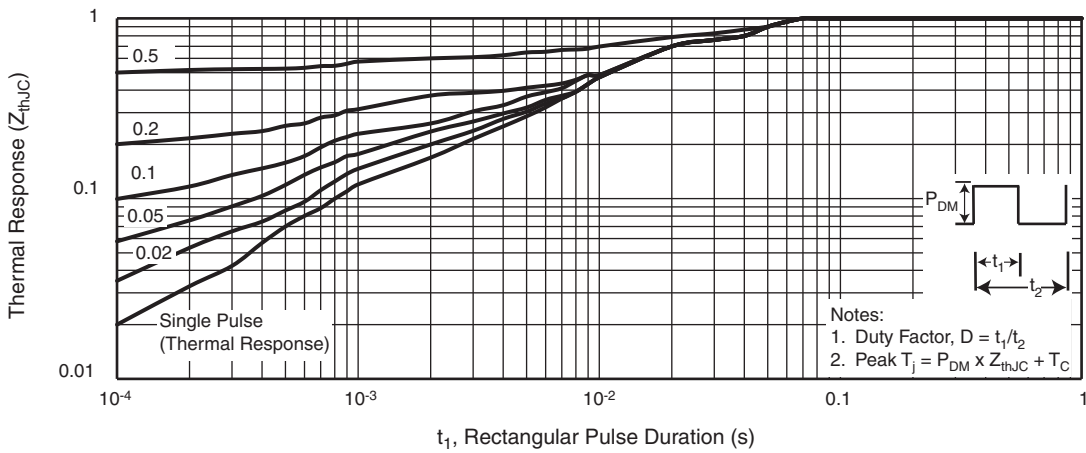


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case (TO-220AB, D²PAK)

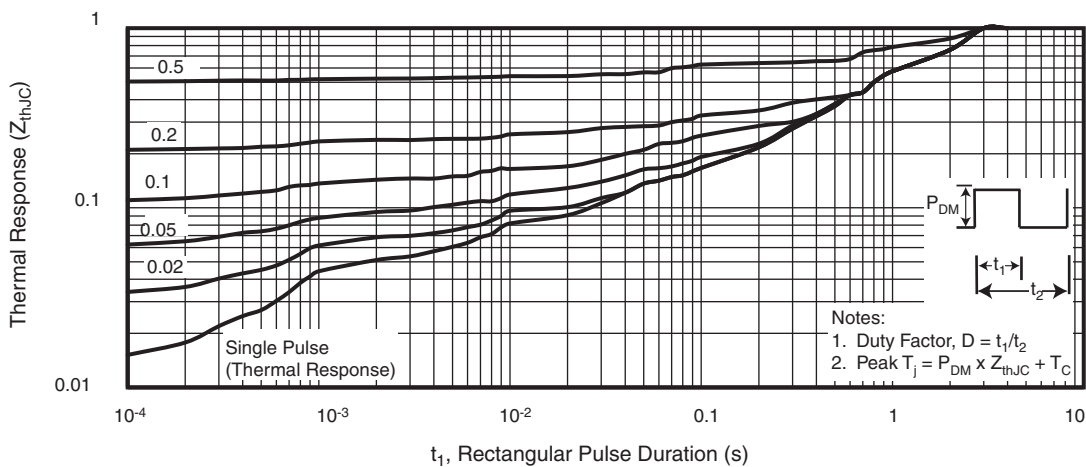


Fig. 12 - Maximum Effective Transient Thermal Impedance, Junction-to-Case (TO-220 FULLPAK)

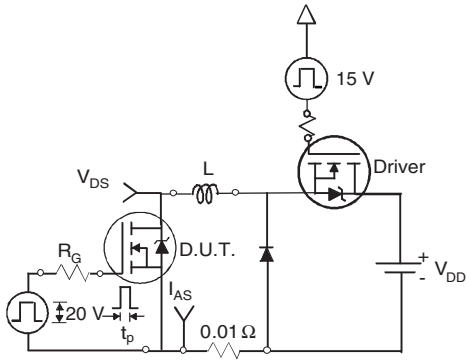


Fig. 13a - Unclamped Inductive Test Circuit

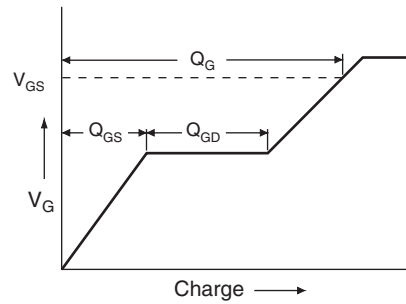


Fig. 14a - Basic Gate Charge Waveform

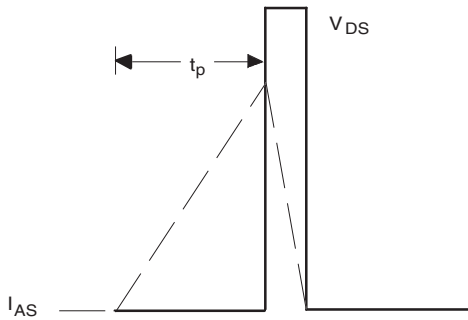


Fig. 13b - Unclamped Inductive Waveforms

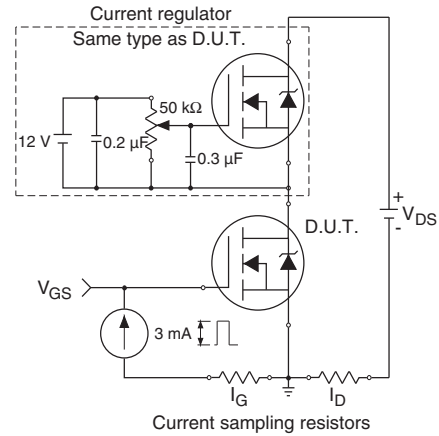
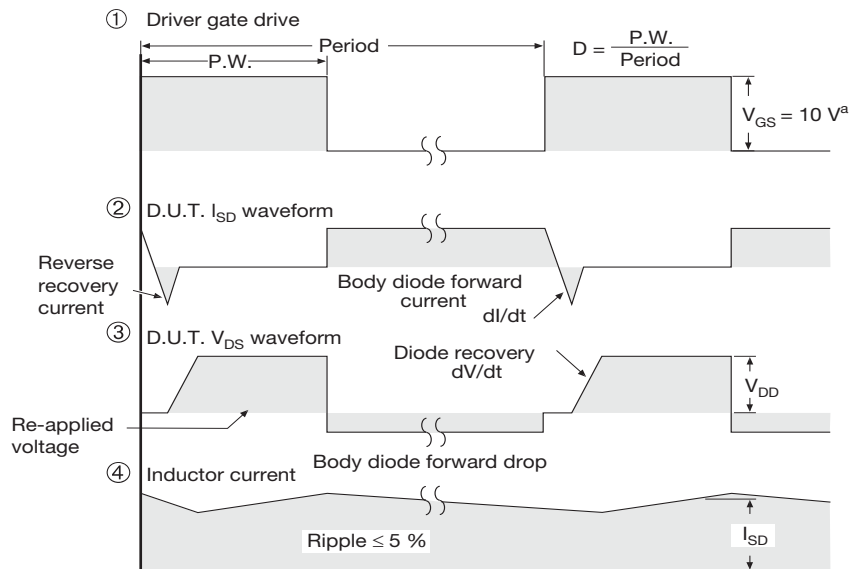
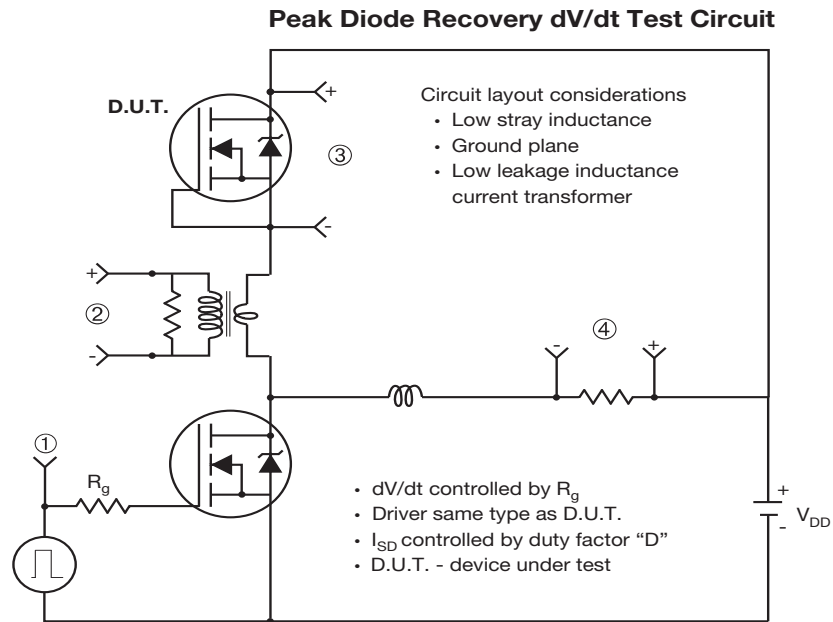


Fig. 14b - Gate Charge Test Circuit



Note

a. $V_{GS} = 5 V$ for logic level devices

Fig. 15 - For N-Channel

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TO-220-1



| DIM. | MILLIMETERS | | INCHES | |
|------|-------------|-------|--------|-------|
| | MIN. | MAX. | MIN. | MAX. |
| A | 4.24 | 4.65 | 0.167 | 0.183 |
| b | 0.69 | 1.02 | 0.027 | 0.040 |
| b(1) | 1.14 | 1.78 | 0.045 | 0.070 |
| c | 0.36 | 0.61 | 0.014 | 0.024 |
| D | 14.33 | 15.85 | 0.564 | 0.624 |
| E | 9.96 | 10.52 | 0.392 | 0.414 |
| e | 2.41 | 2.67 | 0.095 | 0.105 |
| e(1) | 4.88 | 5.28 | 0.192 | 0.208 |
| F | 1.14 | 1.40 | 0.045 | 0.055 |
| H(1) | 6.10 | 6.71 | 0.240 | 0.264 |
| J(1) | 2.41 | 2.92 | 0.095 | 0.115 |
| L | 13.36 | 14.40 | 0.526 | 0.567 |
| L(1) | 3.33 | 4.04 | 0.131 | 0.159 |
| Ø P | 3.53 | 3.94 | 0.139 | 0.155 |
| Q | 2.54 | 3.00 | 0.100 | 0.118 |

ECN: X15-0364-Rev. C, 14-Dec-15
DWG: 6031

Note

- M* = 0.052 inches to 0.064 inches (dimension including protrusion), heatsink hole for HVM





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