NS4215 Data Sheet V1.0

ShenZhen Nsiway Technology Co., Ltd

2013/08

Change History

DATA	VERSION	AUTHOR	CHAGE EXPLAIN

CONTENTS

FIGURE LISTS

TABLE LISTS

General Description

The NS4215 is a stereo, non-clip, filterless, Class-D audio power amplifier. It operates from 5V to 12V supply into 8Ω load. When powered with 12V supply voltage, the NS4215 is capable of delivering 8.5W (per channel) into 8Ω load, with THD+D less than 10%. It operates from 5V to 9V supply into 4Ω load. When powered with 9V supply voltage, the NS4215 is capable of delivering 7.5W (per channel) into 4Ω load, with THD+D less than 10%.
The NS4215 features a non-clip output control,which detects the output clipping caused by the over-level input signal and automatically adjusts the dynamic range of the output signal to prevent the distortion of the audio signal. The non-clip output control also eliminates the output clipping due to a low battery supply voltage.
As a Class-D power amplifier, the NS4215 features high efficiency (up to 80%) and high PSRR (65dB at 217Hz), which make the device ideal for use in cellular handsets and other portable devices.
The NS4215 is available in TSSOP-24 package and is specified over the -40℃ to +85℃ temperature range.

Features

- Non-clip control to suppress output clipping
- Filterless Class-D operation
- High efficiency up to 80%(8Ω load,Po=7W,PVcc=12V)
- Wide Supply Voltage Range Allows Operation from 5 V to 12 V into 8-Ω Stereo Load
- Wide Supply Voltage Range Allows Operation from 5 V to 9 V into 4-Ω Stereo Load
- Output power at 12V supply
  - 7W×2 (8Ω load, 1% THD+N,BTL Output)
  - 8.5W×2 (8Ω load, 10% THD+N,BTL Output)
  - 14W (4Ω load, 1% THD+N,PBTL Output)
  - 17W (4Ω load, 10% THD+N,PBTL Output)
- Output power at 9V supply
  - 4W×2 (8Ω load, 1% THD+N,BTL Output)
  - 5W×2 (8Ω load, 10% THD+N,BTL Output)
  - 6W×2 (4Ω load, 1% THD+N,BTL Output)
  - 7.5W×2 (4Ω load, 10% THD+N,BTL Output)
  - 8W (4Ω load, 1% THD+N,PBTL Output)
  - 10W (4Ω load, 10% THD+N,PBTL Output)
- Low shutdown current: 1μA (typical)
- Short-circuit & thermal protection
- Packages: TSSOP-24

Applications

- Televisions
- Multimedia internet devices

Typical Application Circuit

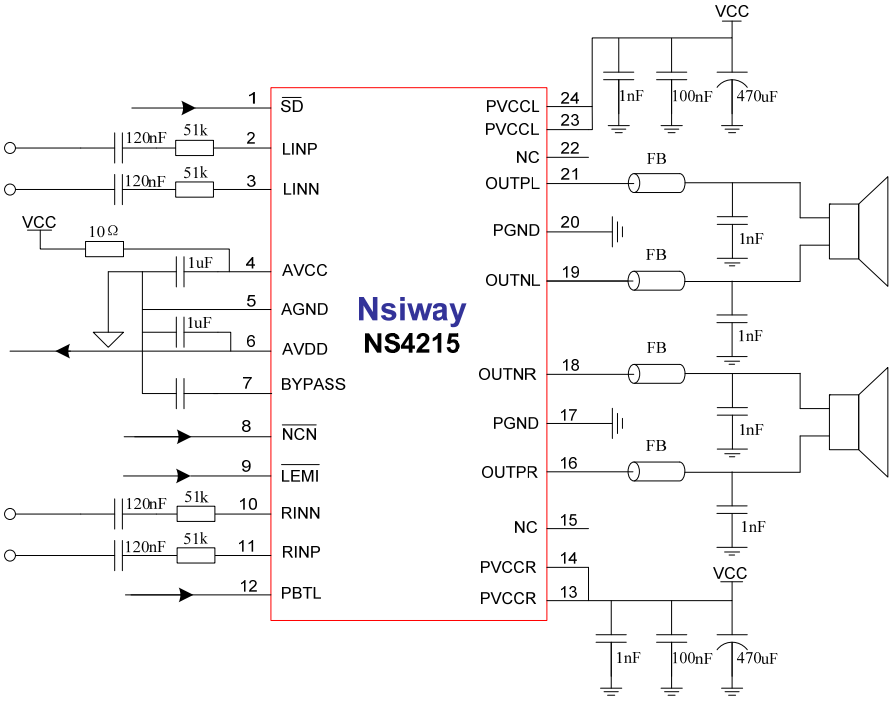


Figure1.NS4215 Typical Application Circuit

Absolute Maximum Ratings

Table1.Absolute Maximum Ratings

Parameter	Min	Max	Unit	Note
Supply Voltage PVCC	5	12.5	V	8-Ω Load BTL Output 4-Ω Load PBTL Output
Supply Voltage PVCC	5	9	V	4-Ω Load BTL Output
/SD	-0.3	PVCC	V	
PBTL	-0.3	PVCC	V	
/LEMI	-0.3	3.3	V	
/NCN	-0.3	3.3	V	
Junction Temperature		125	℃	
Storage Temperature	-65	150	℃	
Lead Temperature (Soldering 10 Seconds0)		260	℃	
Package Thermal Resistance JA		90	℃/W	
Operating Ambient Temperature	-40	85	℃	
ESD Rating		2000	V	Human Body Model
-IT		-150	mA	

Note1: Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Electrical Characteristics

Table2. Electrical Characteristics

PVCC=12V, TA=25°C, AV=36dB, RL=8 Ω, unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Units
PVCC	Supply Voltage	RL=8Ω orRL=4Ω/PBTL	5		12	V
PVCC	Supply Voltage	RL=4Ω/BTL	5		9	V
|VOS|	Output offset voltage	VIN＝0V，Gain=36dB		20		mV
IQ	Quiescent Current	VIN＝0V，No load		22		mA
ISD	Shutdown Current	V/SD =0V		1		μA
PSRR	Power-Supply Rejection Ratio	217Hz		-65		dB
		20KHz		-60		dB
CMRR	Common-Mode Rejection Ratio			-70		dB
fSW	Carrier clock frequency			300		kHz
PO	Output Power （NCNOFF）	THD＝1%,BTL f=1KHz,RL=8Ω,PVCC=12V		7		W
		THD＝10%,BTL f=1KHz,RL=8Ω,PVCC=12V		8.5		W
		THD＝1%,BTL f=1KHz,RL=4Ω,PVCC=9V		6		W
		THD＝10%,BTL f=1KHz,RL=4Ω,PVCC=9V		7.5		W
		THD＝1%,PBTL f=1KHz,RL=4Ω,PVCC=12V		14		W
		THD＝10%,PBTL f=1KHz,RL=4Ω,PVCC=12V		17		W
THD+N	Total Harmonic Distortion Plus Noise	Gain=36dB，f=1kHz RL=8Ω，PO=4W		0.13		%
η	Efficiency	Po=7W,RL =8Ω		80		%
VIH	High–level input voltage		2			V
VIL	Low–level input voltage				0.4	V
tON	Turn-on time			15		ms

tOFF	Turn-off time			2		us
tAT	Attack time			10		ms
tRL	Release time			1.1		s
AVDD	LDO Output		3	3.3	3.5	V
Vn	Output integrated noise	20Hz-20kHz，Gain=20dB		250		uV
SNR	Signal-to-noise ratio	Gain=20dB，f=1kHz RL=8Ω，PO=8W		-80		dB
CS	Over Temperature Hysteresis	Gain=20dB，f=1kHz RL=8Ω，PO=8W		-90		dB
OTP	Over Temperature Protection			150		℃
OTH	Over Temperature Hysteresis			20		℃
AMAX	NCN maximum attenuation gain	NCN Model		-10		dB

Pin Configuration

Pin Layout

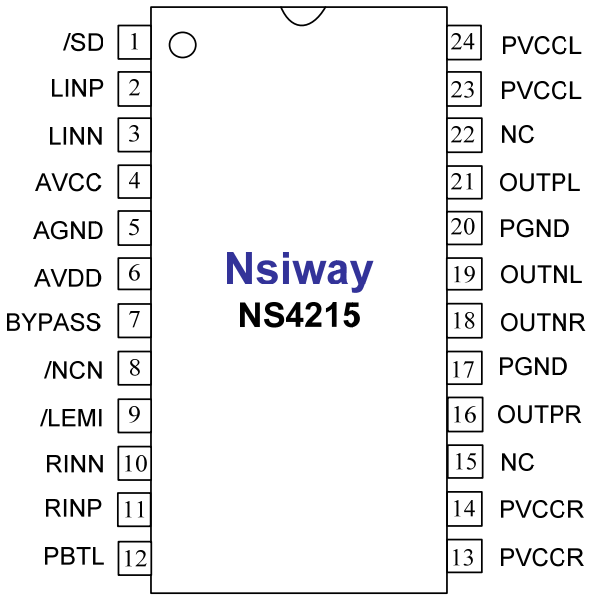


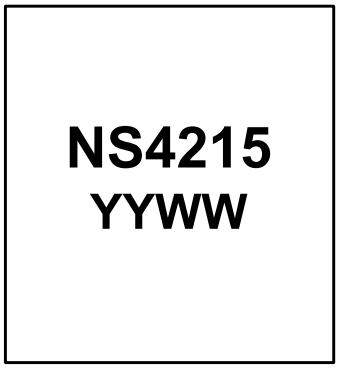
Figure2.NS4215 TSSOP-24 Package(top view)

Pin Discription

Table3. Pin Discription

Pin NO.	Pin Name	Description
1	/SD	Shutdown logic input for audio amp (LOW = outputs Hi-Z, HIGH = outputs enabled).
2	LINP	Positive audio input for left channel.
3	LINN	Negative audio input for left channel.
4	AVCC	Analog supply
5	AGND	Analog signal ground. Connect to the thermal pad.
6	AVDD	3.3V LDO Output
7	BYPASS	Internal analog reference, connect a bypass capacitor from VREF to GND
8	/NCN	non-clip control pin
9	/LEMI	Low EMI control pin
10	RINN	Negative audio input for right channel
11	RINP	Positive audio input for right channel
12	PBTL	Parallel BTL mode switch
13,14	PVCCR	Power supply for right channel H-bridge. Right channel and left channel power supply inputs are connect internally
15	NC	Not connected
16	OUTPR	Class-D H-bridge positive output for right channel.
17	PGND	Power ground for the H-bridges.
18	OUTNR	Class-D H-bridge negative output for right channel.
19	OUTNL	Class-D H-bridge negative output for left channel.
20	PGND	Power ground for the H-bridges.
21	OUTPL	Class-D H-bridge positive output for left channel.
22	NC	Not connected
23,24	PVCCL	Power supply for left channel H-bridge. Right channel and left channel power supply inputs are connect internally.

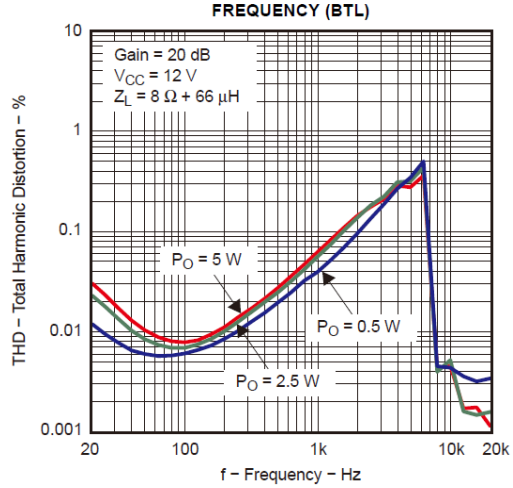
Marking Information



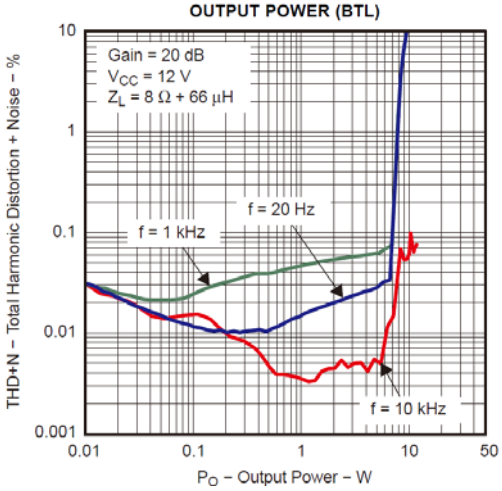
NS: Corporation Code
4215: Partino 4215
YYWW: Date Code

Typical Characteristics

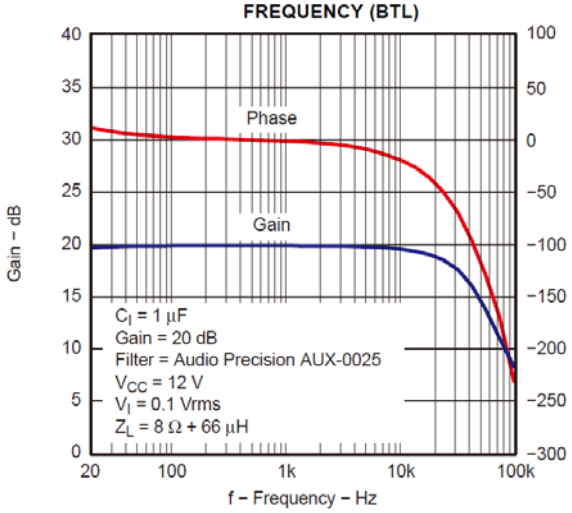
TOTAL HARMONIC DISTORTION
vs
FREQUENCY (BTL)



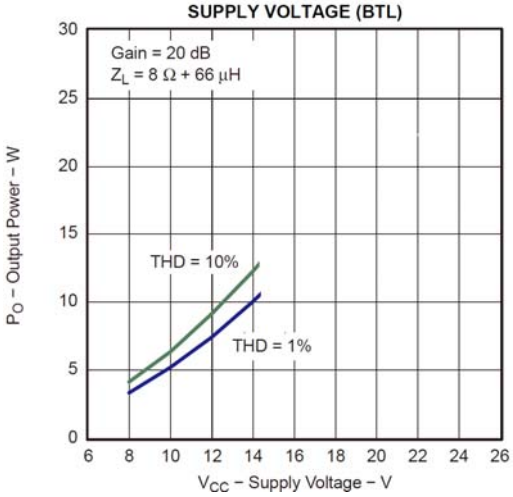
TOTAL HARMONIC DISTORTION + NOISE
vs
OUTPUT POWER (BTL)



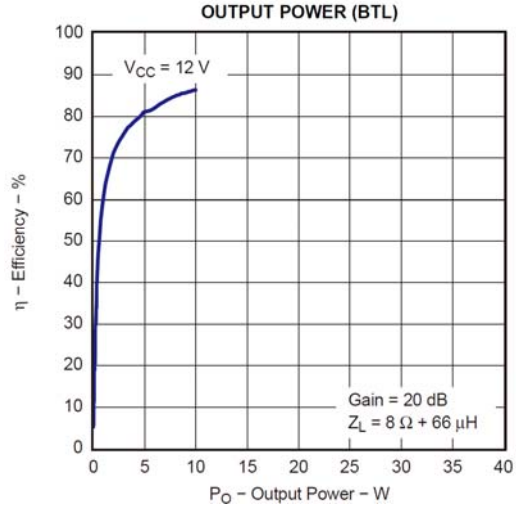
GAIN/PHASE
vs
FREQUENCY (BTL)



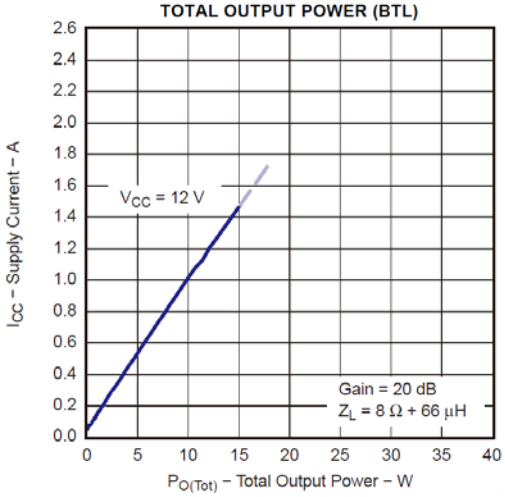
OUTPUT POWER
vs
SUPPLY VOLTAGE (BTL)



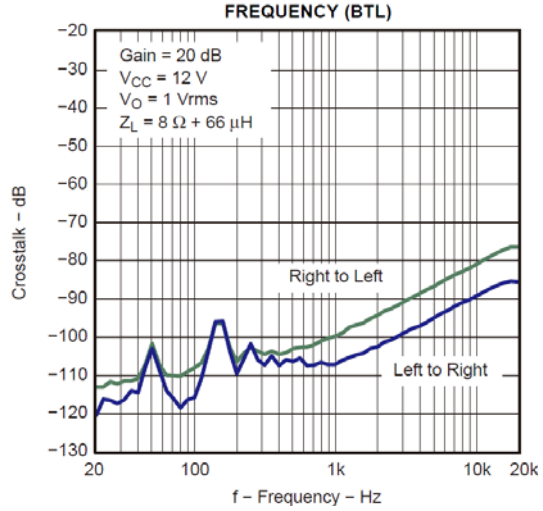
EFFICIENCY
vs
OUTPUT POWER (BTL)



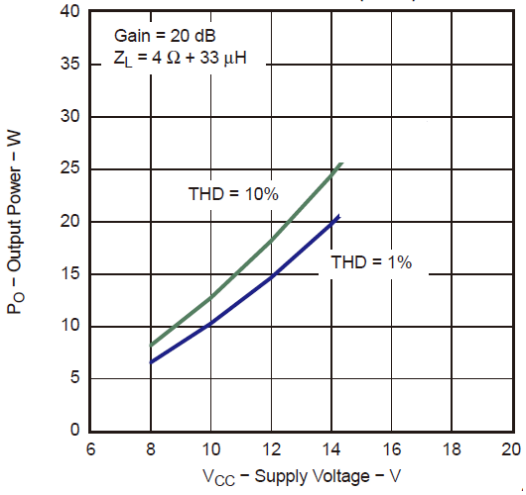
SUPPLY CURRENT
vs
TOTAL OUTPUT POWER (BTL)



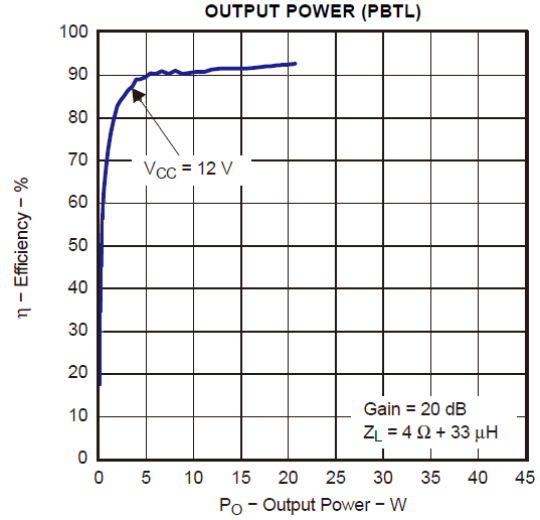
CROSSTALK vs FREQUENCY (BTL)



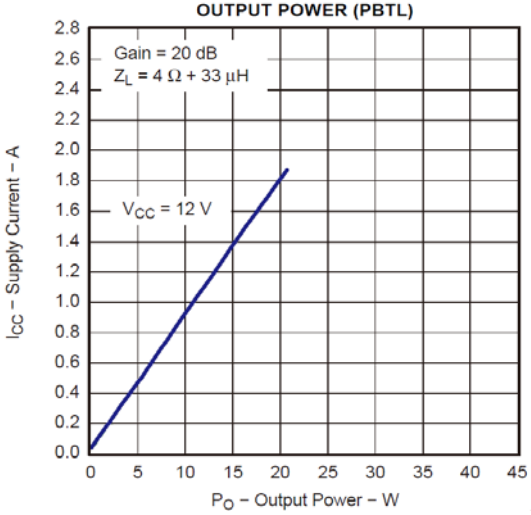
OUTPUT POWER vs SUPPLY VOLTAGE (PBTL)



EFFICIENCY vs OUTPUT POWER (PBTL)



SUPPLY CURRENT vs OUTPUT POWER (PBTL)



Application Information

Block Diagram

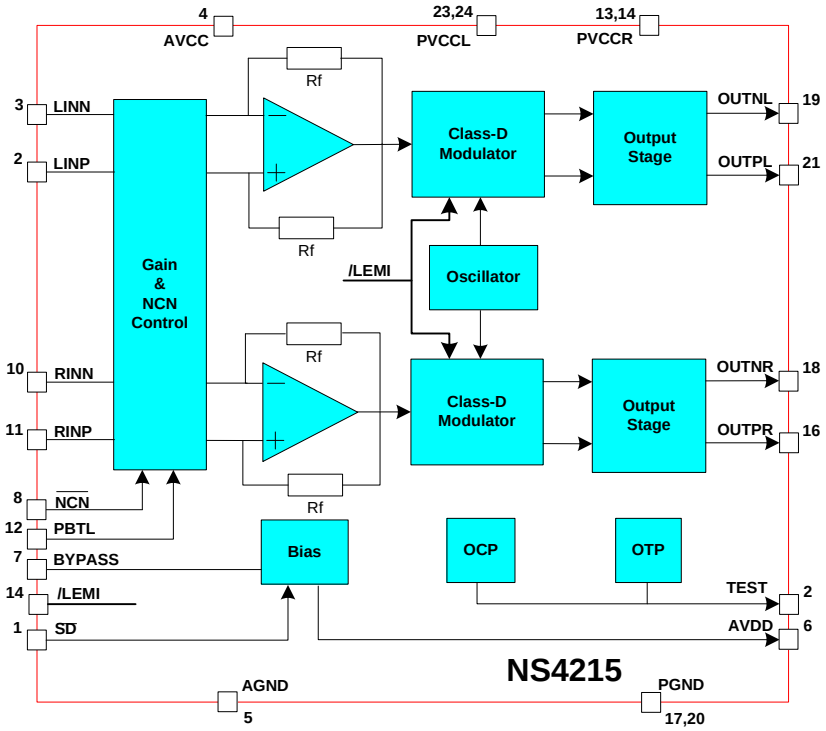


Figure3.The block diagram of NS4215

/SD OPERATION

The NS4215 employs a shutdown mode of operation designed to reduce supply current (ICC) to the absolute minimum level during periods of nonuse for power conservation. The/ SD input terminal should be held high (see specification table for trip point) during normal operation when the amplifier is in use. Pulling/ SD low causes the outputs to mute and the amplifier to enter a low-current state. Never leave/SD unconnected, because amplifier operation would be unpredictable.

For the best power-off pop performance, place the amplifier in the shutdown mode prior to removing the power

Non-Clip(NCN) Control

The non-clip function is to control the output signal level for a maximum output swing without distortion when an excessive input that may cause output clipping is applied. With the non-clip function, the NS4215 lowers the gain of the amplifier to an appropriate value such that the clipping at the outputs is eliminated. It also eliminates the clipping of the output signal due to the decrease of the power-supply voltage. This NCN mode when logic low is placed on the /NCN pin.

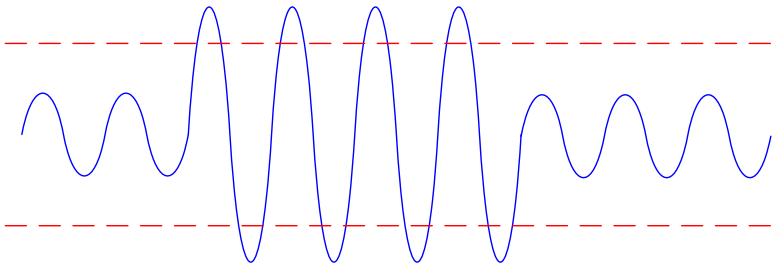


Figure4.Output Signal When Supply Volage is Enough

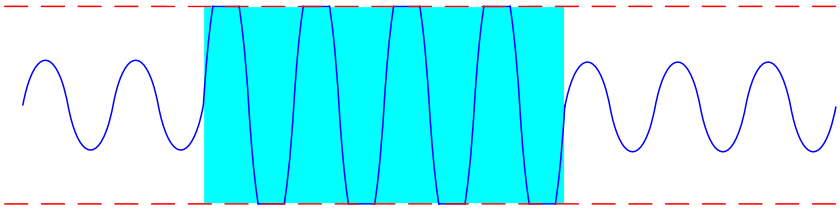


Figure5.Output Signal In NCNOFF Mode

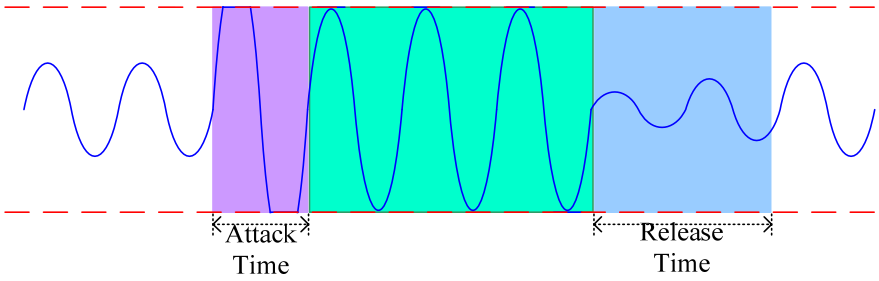


Figure6.Output Signal In NCN Mode

/LEMI OPERATION

NS4215 uses proprietary technology, for the high-frequency transient signals were fully addressed, greatly reduces EMI interference within the whole bandwidth. This Low EMI mode when logic low is placed on the /LEMI pin.

PBTL Select

NS4215 offers the feature of parallel BTL operation with two outputs of each channel connected directly. If the PBTL pin (pin 12) is tied high, the positive and negative outputs of each channel (left and right) are synchronized and in phase. To operate in this PBTL (mono) mode, apply the input signal to the RIGHT input and place the speaker between the LEFT and RIGHT outputs. Connect the positive and negative output together for best efficiency. The voltage slew rate of the PBTL pin must be restricted to no more than 10V/ms. For higher slew rates, use a 100kΩ resistor in series with the terminals. For an example of the PBTL connection, see the schematic in the APPLICATION INFORMATION section.

For normal BTL operation, connect the PBTL pin to local ground.

APPLICATION INFORMATION

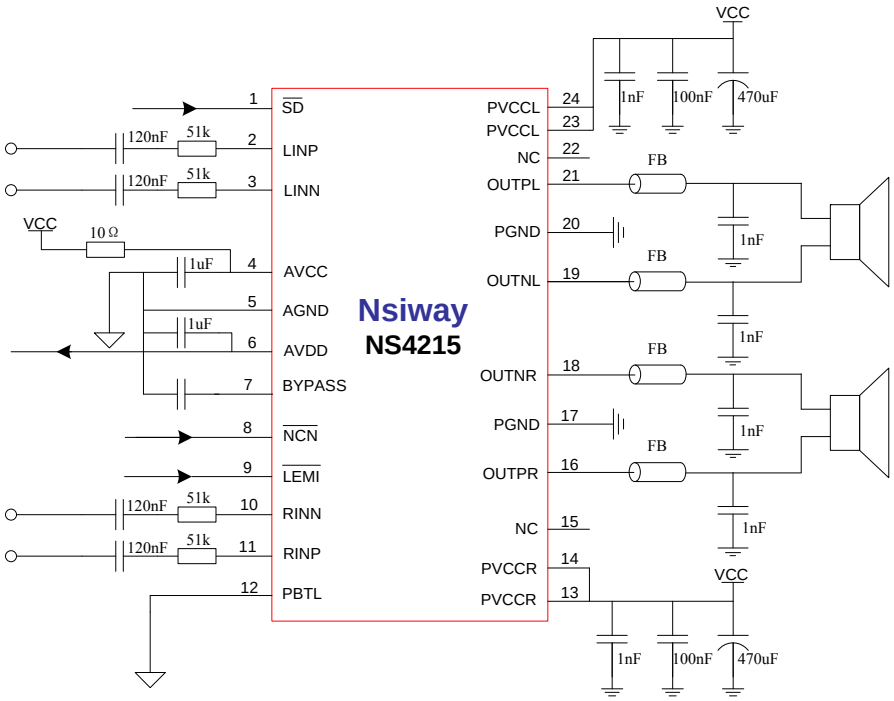


Figure7.Stereo Class-D Amplifier with BTL Output and Differential-Ended Inputs

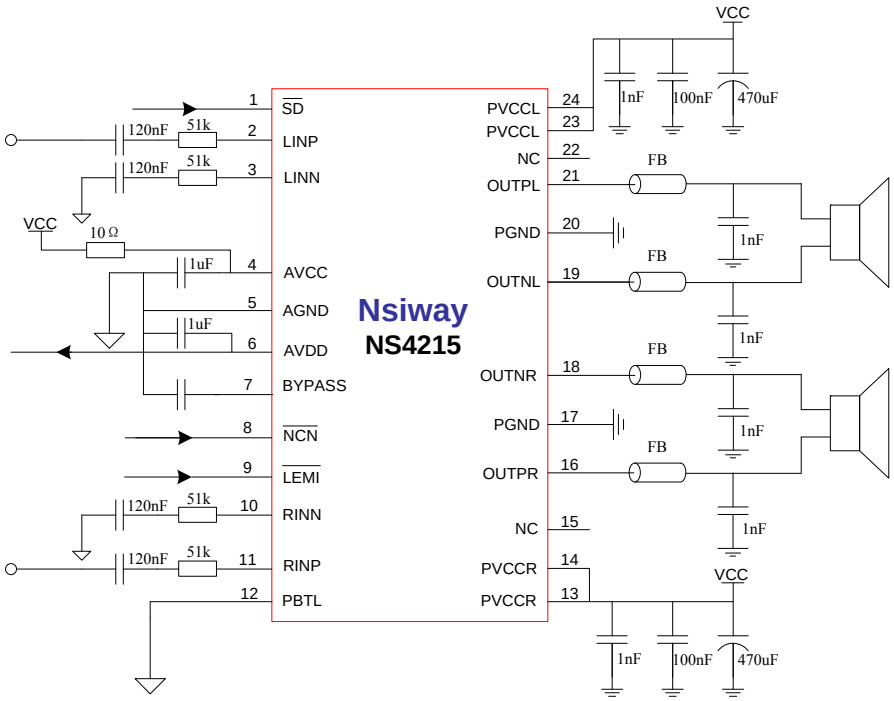


Figure8.Stereo Class-D Amplifier with BTL Output and Single-Ended Inputs

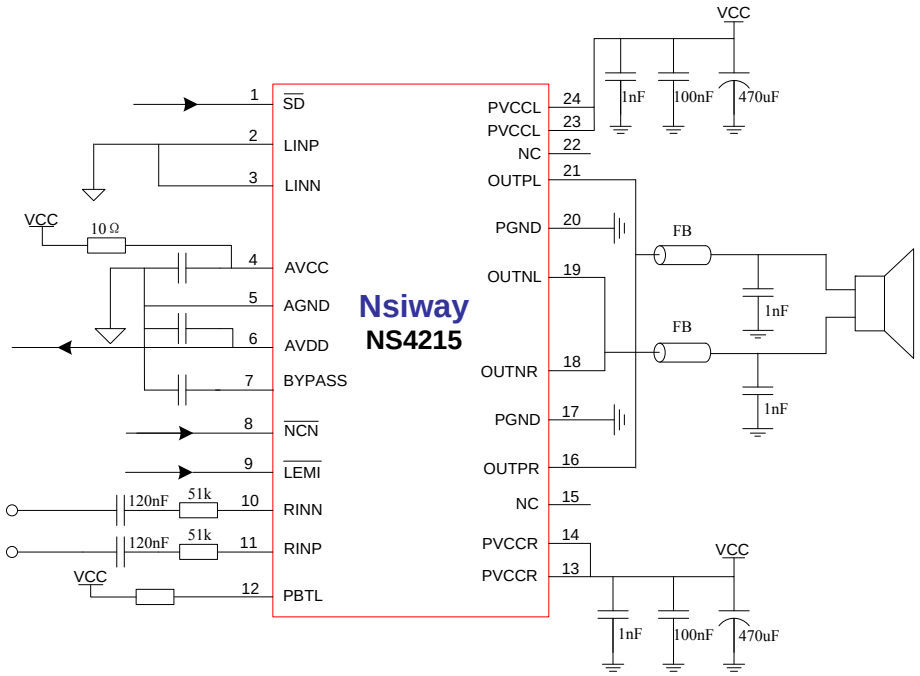


Figure9.Stereo Class-D Amplifier with PBTL Output and Differential-Ended Inputs

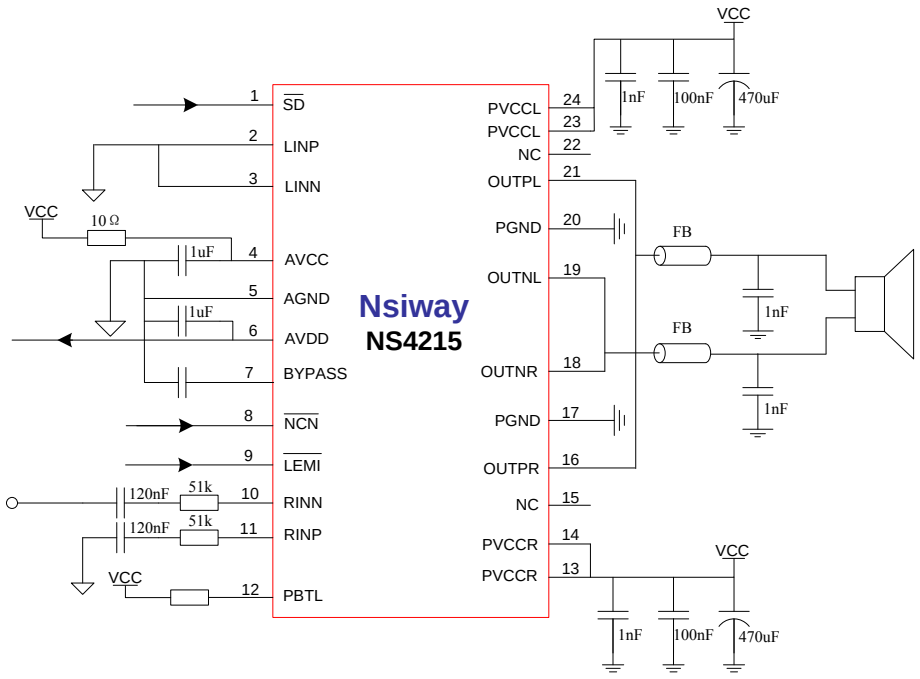


Figure10.Stereo Class-D Amplifier with BTL Output and Single-Ended Inputs

INPUT RESISTANCE

The input resistors (Ri) set the gain of the amplifier according to Equation 1.

$$Av=600k/（9k+Ri）$$

INPUT CAPACITOR, Ci

Changing the gain setting can vary the input resistance of the amplifier from its smallest value. As a result, if a single capacitor is used in the input high-pass filter, the -3 dB or cutoff frequency may change when changing gain steps.

$$fc=1/(2\pi \times Zi \times Ci)$$

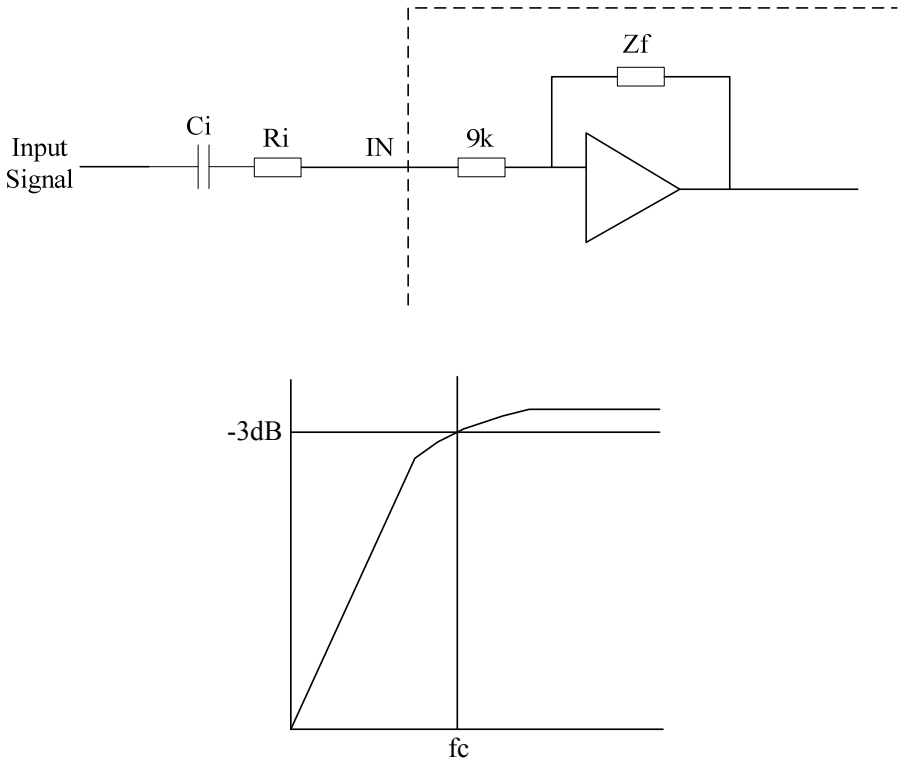


Figure11.highpass filter

The value of CI is important, as it directly affects the bass (low-frequency) performance of the circuit. Consider the example where ZI is 60 kΩ and the specification calls for a flat bass response down to 20 Hz. In this example, CI is 0.13 µF; so, one would likely choose a value of 0.15 µF as this value is commonly used.

POWER SUPPLY DECOUPLING, Cs

The NS4215 is a high-performance CMOS audio amplifier that requires adequate power supply decoupling to ensure that the output total harmonic distortion (THD) is as low as possible. Power supply decoupling also prevents oscillations for long lead lengths between the amplifier and the speaker. Optimum decoupling is achieved by using a network of capacitors of different types that target specific types of noise on the power supply leads. For higher frequency transients due to parasitic circuit elements such as bond wire and copper trace inductances as well as lead frame capacitance, a good quality low equivalent-series-resistance (ESR) ceramic capacitor of value between 220 pF and 1000 pF works well. This capacitor should be placed as close to the device PVCC pins and system ground (either PGND pins or PowerPad) as possible. For mid-frequency noise due to filter resonances or

PWM switching transients as well as digital hash on the line, another good quality capacitor typically 0.1 µF to 1 µF placed as close as possible to the device PVCC leads works best For filtering lower frequency noise signals, a larger aluminum electrolytic capacitor of 220 µF or greater placed near the audio power amplifier is recommended. The 220 µF capacitor also serves as a local storage capacitor for supplying current during large signal transients on the amplifier outputs. The PVCC terminals provide the power to the output transistors, so a 220 µF or larger capacitor should be placed on each PVCC terminal. A 10 µF capacitor on the AVCC terminal is adequate. Also, a small decoupling resistor between AVCC and PVCC can be used to keep high frequency class D noise from entering the linear input amplifiers.

When to Use an Output Filter for EMI Suppression

The NS4215 has been tested with a simple ferrite bead filter for a variety of applications including long speaker wires up to 125 cm and high power. The NS4215 EVM passes FCC Class B specifications under these conditions using twisted speaker wires. The size and type of ferrite bead can be selected to meet application requirements. Also, the filter capacitor can be increased if necessary with some impact on efficiency.

There may be a few circuit instances where it is necessary to add a complete LC reconstruction filter. These circumstances might occur if there are nearby circuits which are sensitive to noise. In these cases a classic second order Butterworth filter similar to those shown in the figures below can be used.

Some systems have little power supply decoupling from the AC line but are also subject to line conducted interference (LCI) regulations. These include systems powered by "wall warts" and "power bricks." In these cases, it LC reconstruction filters can be the lowest cost means to pass LCI tests. Common mode chokes using low frequency ferrite material can also be effective at preventing line conducted interference.

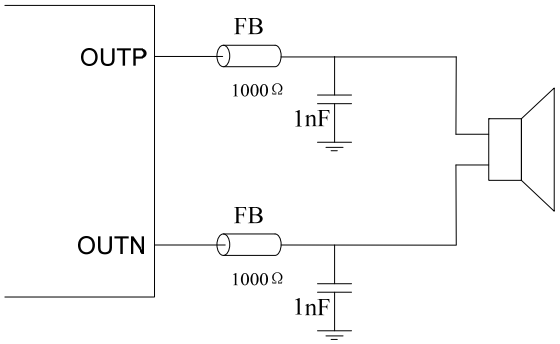


Figure12. Typical Ferrite Chip Bead Filter (Chip Bead Example:)

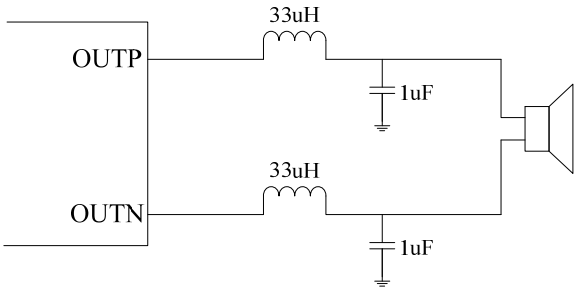


Figure13. Typical LC Output Filter, Cutoff Frequency of 27 kHz, Speaker Impedance = 8 Ω

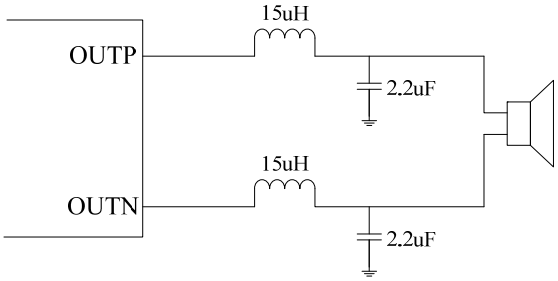


Figure14.Typical LC Output Filter, Cutoff Frequency of 27 kHz, Speaker Impedance = 4 Ω

PRINTED-CIRCUIT BOARD (PCB) LAYOUT

The NS4215 can be used with a small, inexpensive ferrite bead output filter for most applications. However, since the Class-D switching edges are fast, it is necessary to take care when planning the layout of the printed circuit board. The following suggestions will help to meet EMC requirements.

Decoupling capacitors—The high-frequency decoupling capacitors should be placed as close to the PVCC and AVCC terminals as possible. Large (220 µF or greater) bulk power supply decoupling capacitors should be placed near the NS4215 on the PVCCL and PVCCR supplies. Local, high-frequency bypass capacitors should be placed as close to the PVCC pins as possible. These caps can be connected to the thermal pad directly for an excellent ground nnecticoon. Consider adding a small, good quality low ESR ceramic capacitor between 220 pF and 1000 pF and a larger mid-frequency cap of value between 0.1µF and 1µF also of good quality to the PVCC connections at each end of the chip.

Keep the current loop from each of the outputs through the ferrite bead and the small filter cap and back to PGND as small and tight as possible. The size of this current loop determines its effectiveness as an antenna.

Grounding—The AVCC (pin 7) decoupling capacitor should be grounded to analog ground (AGND). The PVCC decoupling capacitors should connect to PGND. Analog ground and power ground should be connected at the thermal pad, which should be used as a central ground connection or star ground for the NS4215.

Test Setup for Performance Testing

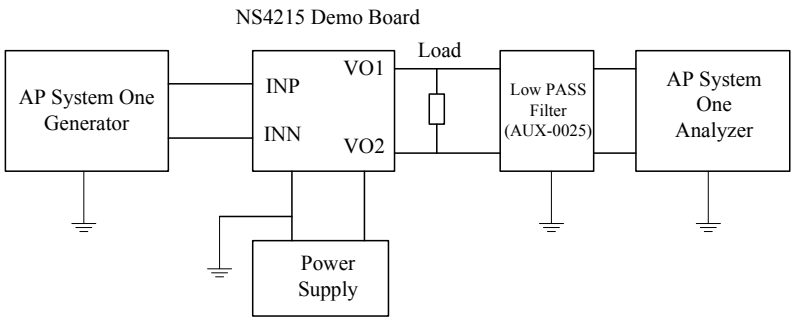


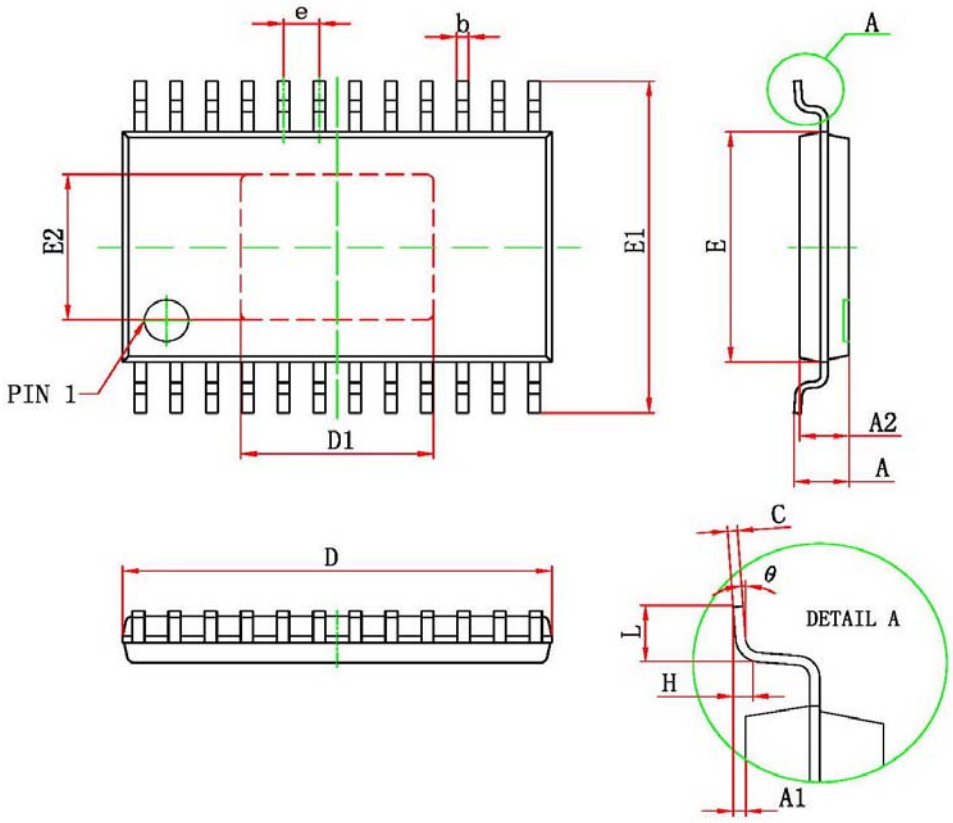
Figure15.Typical Testing Circuit

Notes

1. The AP AUX-0025 low pass filter is necessary for class-D amplifier measurement with AP analyzer.
2. Two33µH inductors are used in series with load resistor to emulate the small speaker for efficiency measurement.

Physical Dimensions

TSSOP24/PP PACKAGE OUTLINE DIMENSIONS



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
D	7.700	7.900	0.303	0.311
D1	3.950	4.150	0.156	0.163
E	4.300	4.500	0.169	0.177
b	0.190	0.300	0.007	0.012
c	0.090	0.200	0.004	0.008
E1	6.250	6.550	0.246	0.258
E2	2.750	2.950	0.108	0.116
A		1.100		0.043
A2	0.800	1.000	0.031	0.039
A1	0.020	0.150	0.001	0.006
e	0.65 (BSC)		0.026 (BSC)	
L	0.500	0.700	0.020	0.028
H	0.25(TYP)		0.01(TYP)	
θ	1°	7°	1°	7°

Figure16.The Package of TSSOP-24

Notice：Shenzhen Nsiway Co. LTD. Reserve the right to modify the datasheet at anytime,and without notice, Only Shenzhen Nsiway Co. LTD. have the right to explain the content in this datasheet.