

## DM54LS273/DM74LS273 8-Bit Register with Clear

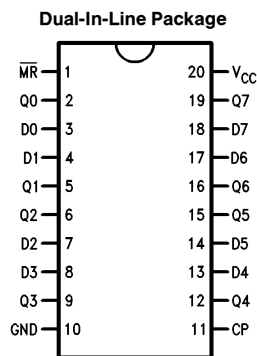
### General Description

The <sup>+</sup>LS273 is a high speed 8-bit register, consisting of eight D-type flip-flops with a common Clock and an asynchronous active LOW Master Reset. This device is supplied in a 20-pin package featuring 0.3 inch row spacing.

### Features

- Edge-triggered
- 8-bit high speed register
- Parallel in and out
- Common clock and master reset

### Connection Diagram



TL/F/9825-1

**Order Number DM54LS273E, DM54LS273J,  
DM54LS273W, DM74LS273M or DM74LS273N  
See NS Package Number E20A, J20A, M20B,  
N20A or W20A**

Pin Names	Description
CP	Clock Pulse Input (Active Rising Edge)
D0–D7	Data Inputs
$\overline{\text{MR}}$	Asynchronous Master Reset Input (Active LOW)
Q0–Q7	Flip-Flop Outputs

## Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54LS	-55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	-65°C to +150°C

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

## Recommended Operating Conditions

Symbol	Parameter	DM54LS273			DM74LS273			Units
		Min	Nom	Max	Min	Nom	Max	
V <sub>CC</sub>	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V <sub>IH</sub>	High Level Input Voltage	2			2			V
V <sub>IL</sub>	Low Level Input Voltage			0.7			0.8	V
I <sub>OH</sub>	High Level Output Current			-0.4			-0.4	mA
I <sub>OL</sub>	Low Level Output Current			4			8	mA
T <sub>A</sub>	Free Air Operating Temperature	-55		125	0		70	°C
t <sub>s</sub> (H) t <sub>s</sub> (L)	Setup Time HIGH or LOW D <sub>n</sub> to CP	15			15			ns
t <sub>h</sub> (H) t <sub>h</sub> (L)	Hold Time HIGH or LOW D <sub>n</sub> to CP	5			5			ns
t <sub>w</sub> (H) t <sub>w</sub> (L)	CP Pulse Width HIGH or LOW	20			20			ns
t <sub>w</sub> (L)	M <sub>FR</sub> Pulse Width LOW	20			20			ns
t <sub>rec</sub>	Recovery Time M <sub>FR</sub> to CP	15			15			ns

## Electrical Characteristics

Over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 1)	Max	Units
V <sub>I</sub>	Input Clamp Voltage	V <sub>CC</sub> = Min, I <sub>I</sub> = -18 mA			-1.5	V
V <sub>OH</sub>	High Level Output Voltage	V <sub>CC</sub> = Min, I <sub>OH</sub> = Max, V <sub>IL</sub> = Max	DM54 2.5			V
			DM74 2.7	3.4		
V <sub>OL</sub>	Low Level Output Voltage	V <sub>CC</sub> = Min, I <sub>OL</sub> = Max, V <sub>IH</sub> = Min	DM54		0.4	V
			DM74	0.35	0.5	
		I <sub>OL</sub> = 4 mA, V <sub>CC</sub> = Min	DM74	0.25	0.4	
I <sub>I</sub>	Input Current @ Max Input Voltage	V <sub>CC</sub> = Max, V <sub>I</sub> = 7V V <sub>I</sub> = 10V (DM54)			0.1	mA
I <sub>IH</sub>	High Level Input Current	V <sub>CC</sub> = Max, V <sub>I</sub> = 2.7V			20	μA
I <sub>IL</sub>	Low Level Input Current	V <sub>CC</sub> = Max, V <sub>I</sub> = 0.4V			-0.4	mA
I <sub>OS</sub>	Short Circuit Output Current	V <sub>CC</sub> = Max (Note 2)	DM54 -20		-100	mA
			DM74 -20		-100	
I <sub>CC</sub>	Supply Current	V <sub>CC</sub> = Max			27	mA

Note 1: All typicals are at V<sub>CC</sub> = 5V, T<sub>A</sub> = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.



## Switching Characteristics $V_{CC} = +5.0V, T_A = +25^\circ C$

Symbol	Parameter	$C_L = 15 \text{ pF}$				Units
		DM54LS		DM74LS		
		Min	Max	Min	Max	
$f_{max}$	Maximum Clock Frequency	30		30		MHz
$t_{PLH}$ $t_{PHL}$	Propagation Delay CP to $Q_n$		24		24	ns
$t_{PLH}$	Propagation Delay $\overline{MR}$ to $Q_n$		27		27	ns

## Functional Description

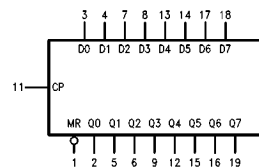
The  $\text{LS273}$  is an 8-bit parallel register with a common Clock and common Master Reset. When the  $\overline{MR}$  input is LOW, the Q outputs are LOW, independent of the other inputs. Information meeting the setup and hold time requirements of the D inputs is transferred to the Q outputs on the LOW-to-HIGH transition of the clock input.

## Truth Table

MR	Inputs		Outputs $Q_n$
	CP	$D_n$	
L	X	X	L
H		H	H
H		L	L

H = HIGH Voltage Level  
L = LOW Voltage Level  
X = Immaterial

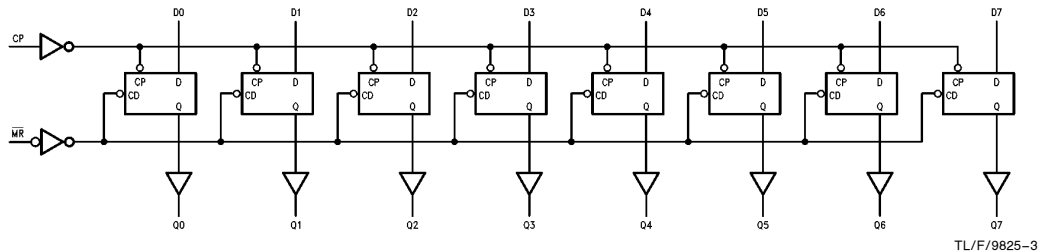
## Logic Symbol



TL/F/9825-2

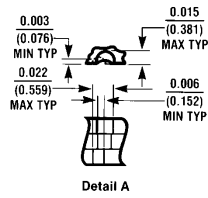
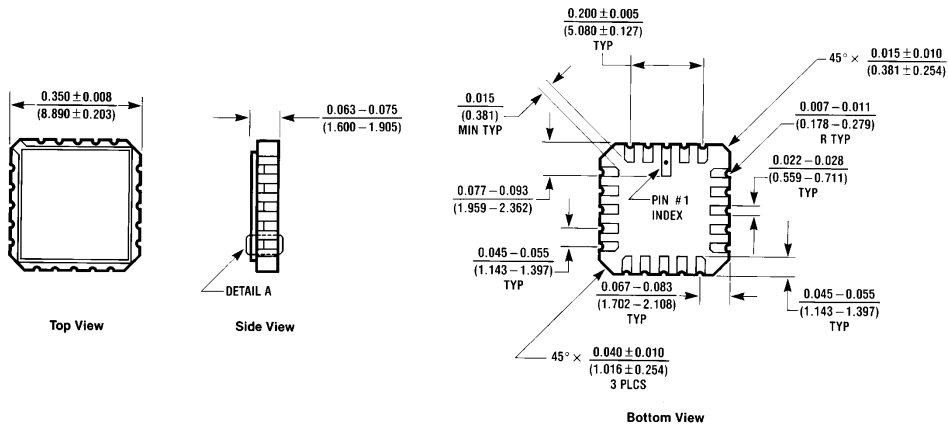
$V_{CC}$  = Pin 20  
GND = Pin 10

## Logic Diagram



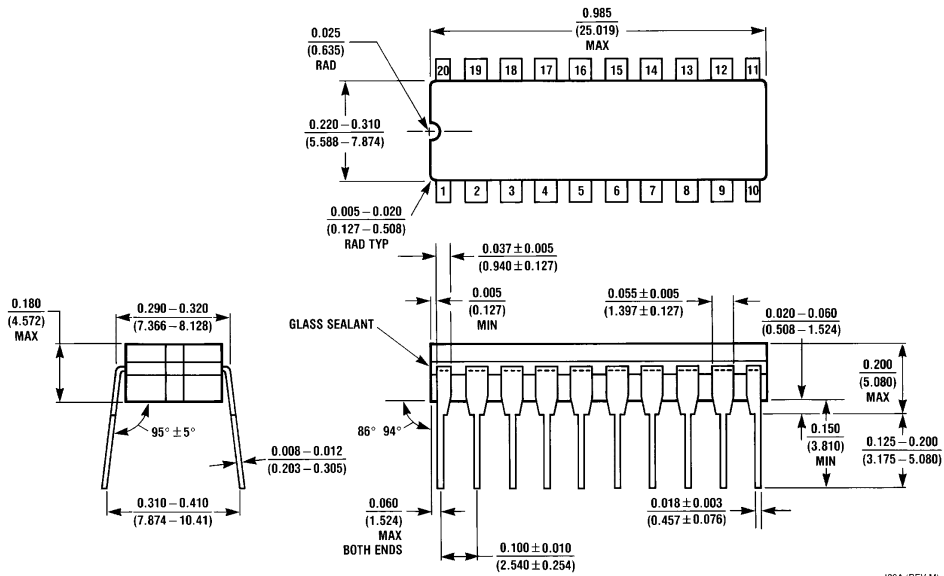
TL/F/9825-3

**Physical Dimensions** inches (millimeters)



**Ceramic Leadless Chip Carrier Package (E)**  
 Order Number DM54LS273E  
 NS Package Number E20A

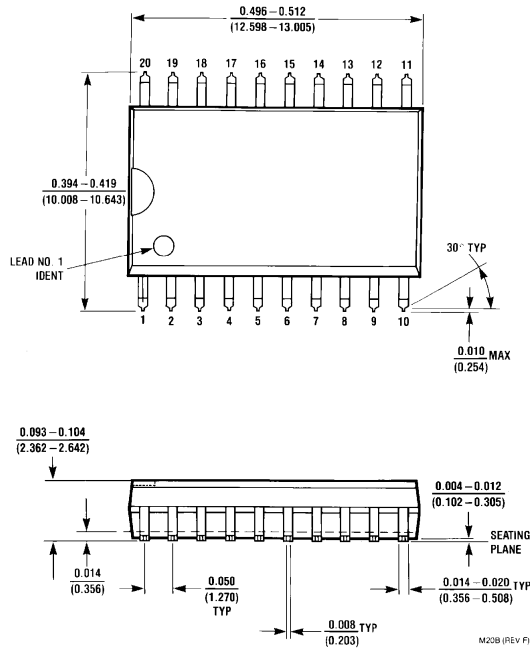
E20A (REV D)



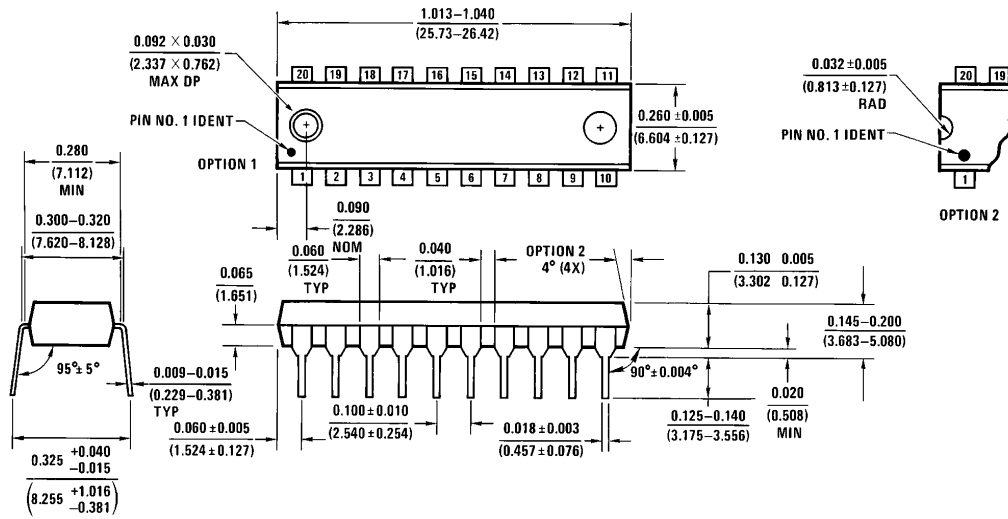
**20-Lead Ceramic Dual-In-Line Package (J)**  
 Order Number DM54LS273J  
 NS Package Number J20A

J20A (REV M)

**Physical Dimensions** inches (millimeters) (Continued)

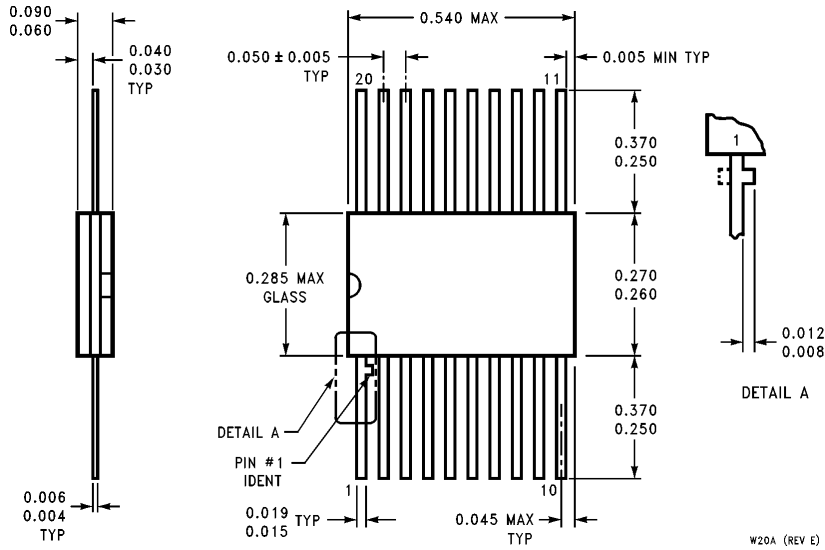


**20-Lead Wide Small Outline Molded Package (M)**  
**Order Number DM74LS273M**  
**NS Package Number M20B**



**20-Lead Molded Dual-In-Line Package (N)**  
**Order Number DM74LS273N**  
**NS Package Number N20A**

**Physical Dimensions** inches (millimeters) (Continued)



**20-Lead Ceramic Flat Package (W)**  
**Order Number DM54LS273W**  
**NS Package Number W20A**

W20A (REV E)

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