

ME15N10/ME15N10-G

N-Channel 100-V (D-S) MOSFET

GENERAL DESCRIPTION

The ME15N10 is the N-Channel logic enhancement mode power field effect transistors, using high cell density, DMOS trench technology. This high density process is especially tailored to minimize on state resistance. These devices are particularly suited for low voltage application such as cellular phone, notebook computer power management and other battery powered circuits, and low in-line power loss that are needed in a very small outline surface mount package.

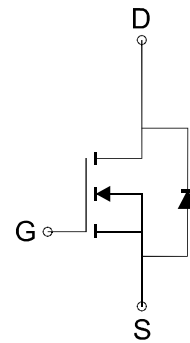
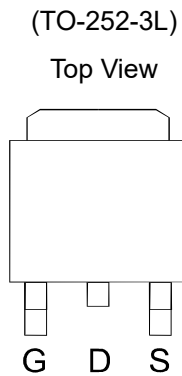
FEATURES

- $R_{DS(ON)} \square 100m\Omega @V_{GS}=10V$
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability

APPLICATIONS

- Power Management in Note book
- DC/DC Converter
- Load Switch
- LCD Display inverter

PIN CONFIGURATION



N-Channel MOSFET

Ordering Information: ME15N10 (Pb-free)

ME15N10-G (Green product-Halogen free)

Absolute Maximum Ratings (TA=25°C Unless Otherwise Noted)

Parameter	Symbol	Rating	Unit
Drain-Source Voltage	V_{DSS}	100	V
Gate-Source Voltage	V_{GSS}	± 20	V
Continuous Drain Current (Tj=150°C)	I_D	$T_C=25^\circ C$	14.7
		$T_C=70^\circ C$	13.6
Pulsed Drain Current	I_{DM}	59	A
Maximum Power Dissipation	P_D	$T_C=25^\circ C$	34.7
		$T_C=70^\circ C$	22.2
Operating Junction Temperature	T_J	-55 to 150	°C
Thermal Resistance-Junction to Case *	$R_{\theta JC}$	3.6	°C/W

* The device mounted on 1in² FR4 board with 2 oz copper

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Electrical Characteristics (T_A=25°C Unless Otherwise Specified)

Symbol	Parameter	Limit	Min	Typ	Max	Unit
STATIC						
B _V DSS	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =250μ A	100			V
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =250μ A	1		3	V
I _{GSS}	Gate Leakage Current	V _{DS} =0V, V _{GS} =±20V			±100	nA
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =80V, V _{GS} =0V			1	μ A
R _{DS(ON)}	Drain-Source On-Resistance ^a	V _{GS} =10V, I _D = 8A		80	100	mΩ
V _{SD}	Diode Forward Voltage	I _S =8A, V _{GS} =0V		0.9	1.2	V
DYNAMIC						
Q _g	Total Gate Charge	V _{DS} =80V, V _{GS} =10V, I _D =10A		24		nC
Q _g	Total Gate Charge	V _{DS} =80V, V _{GS} =4.5V, I _D =10A		13		
Q _{gs}	Gate-Source Charge			4.6		
Q _{gd}	Gate-Drain Charge			7.6		
C _{iss}	Input Capacitance	V _{DS} =15V, V _{GS} =0V, f=1MHz		890		pF
C _{oss}	Output Capacitance			58		
C _{rss}	Reverse Transfer Capacitance			23		
R _g	Gate-Resistance	V _{DS} =0V, V _{GS} =0V, f=1MHz		0.9		Ω
t _{d(on)}	Turn-On Delay Time	V _{DS} =50V, R _L =5Ω , V _{GEN} =10V, R _G =1Ω		14		ns
t _r	Turn-On Rise Time			33		
t _{d(off)}	Turn-Off Delay Time			39		
t _f	Turn-Off Fall Time			5		

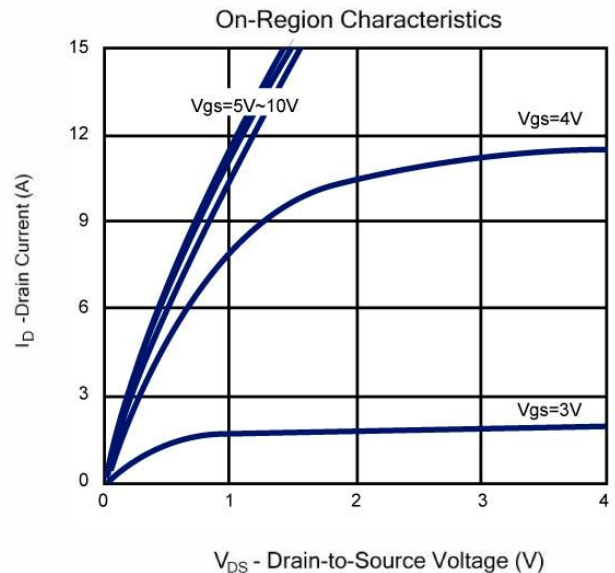
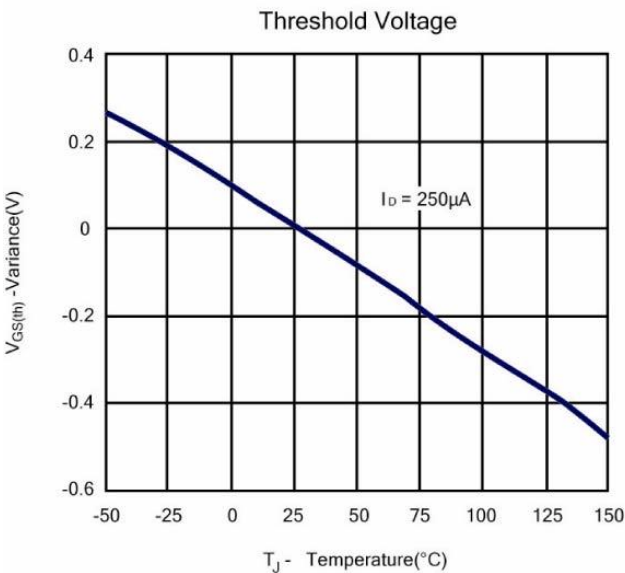
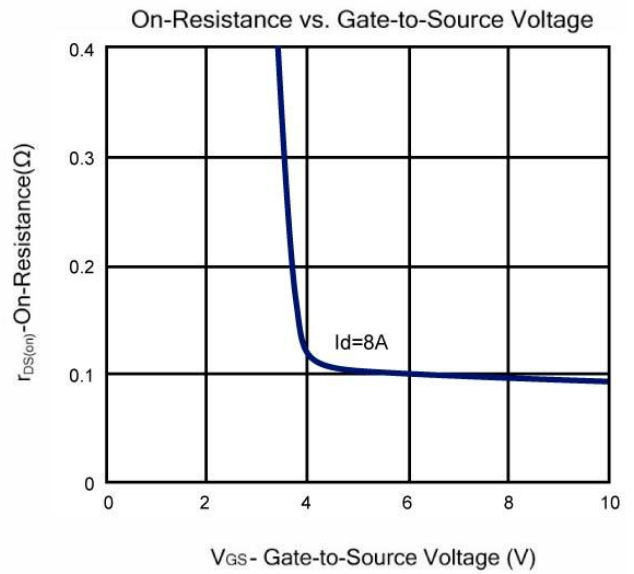
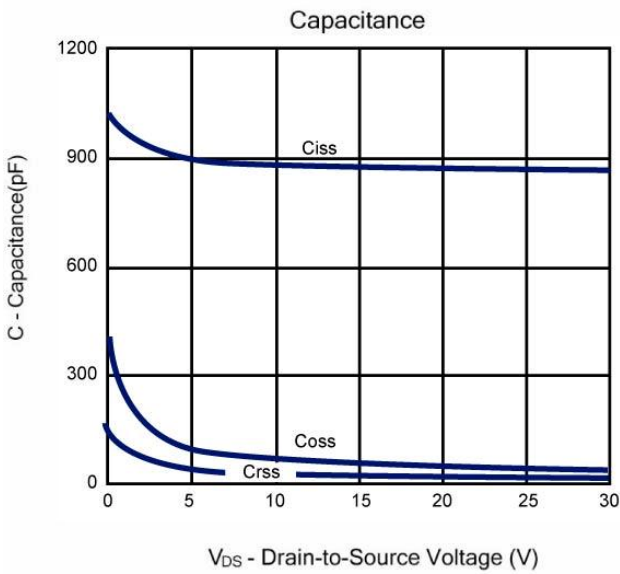
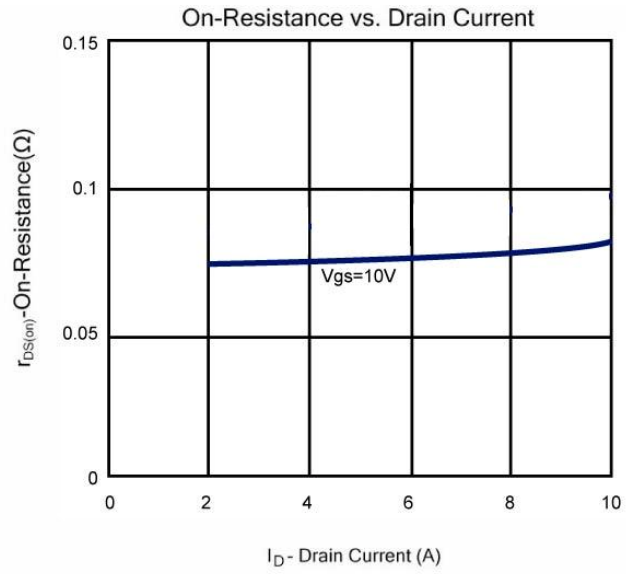
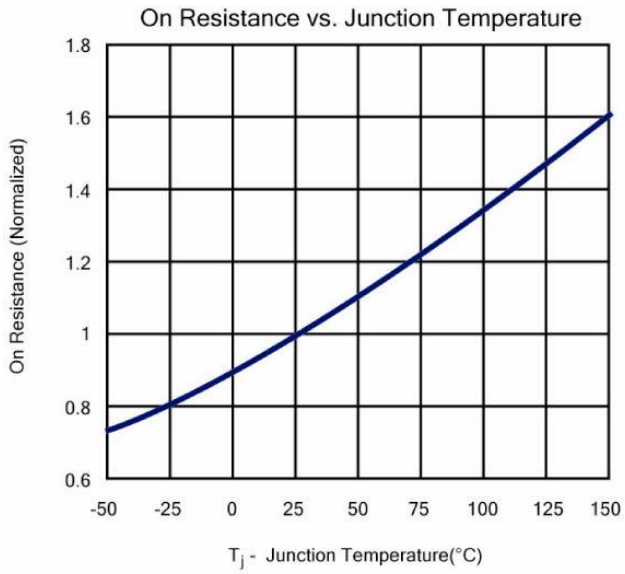
Notes: a. Pulse test: pulse width □ 300us, duty cycle □ 2%, Guaranteed by design, not subject to production testing.

b. Matsuki reserves the right to improve product design, functions and reliability without notice.

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Typical Characteristics (T_J = 25°C Noted)



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