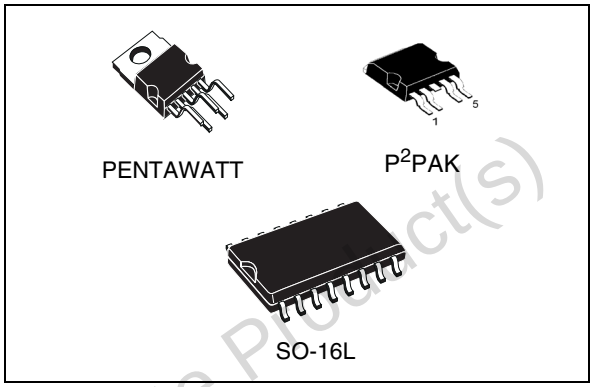
VN920

Single channel high-side solid-state relay

Features

Type	$R_{DS(on)}$	I_{OUT}	V_{CC}
VN920 VN920-B5 VN920SO	16 mΩ	30 A	36 V

- CMOS compatible input
- Proportional load current sense
- Shorted load protection
- Under-voltage and over-voltage shutdown
- Over-voltage clamp
- Thermal shutdown
- Current limitation
- Protection against loss of ground and loss of V_{CC}
- Very low standby power dissipation
- Reverse battery protected (see *Application schematic*)



Description

The VN920 is a monolithic device designed in STMicroelectronics VIPower M0-3 technology. The VN920 is intended for driving any type of load with one side connected to ground. The active V_{CC} pin voltage clamp protects the device against low energy spikes (see ISO7637 transient compatibility table). Active current limitation combined with thermal shutdown and automatic restart protects the device against over-load.

The device integrates an analog current sense output which delivers a current proportional to the load current. The device automatically turns off in the case where the ground pin becomes disconnected.

Table 1. Device summary

Package	Order codes	
	Tube	Tape and reel
PENTAWATT	VN920	-
P²PAK	VN920-B5	VN920-B513TR
SO-16L	VN920SO	VN920SO13TR

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1 Block diagram and pin description

Figure 1. Block diagram

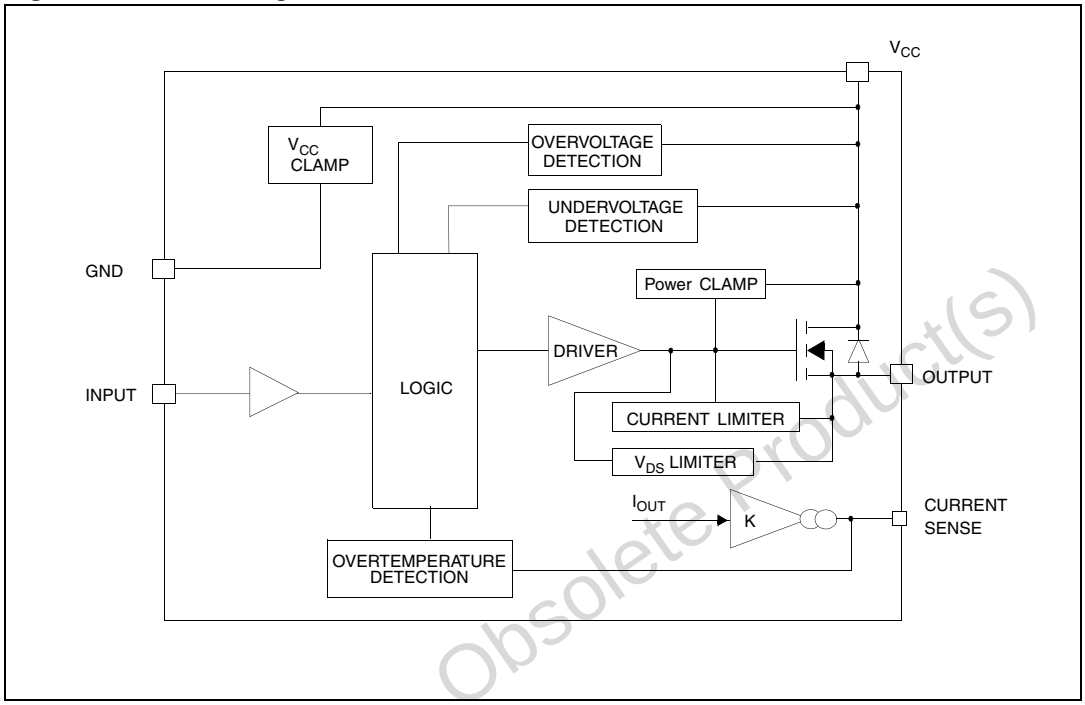
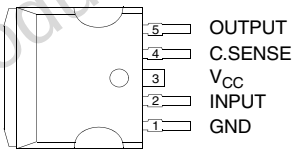
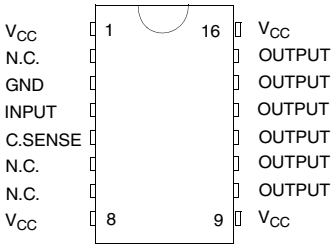


Figure 2. Configuration diagram (top view)



P2PAK/ PENTAWATT



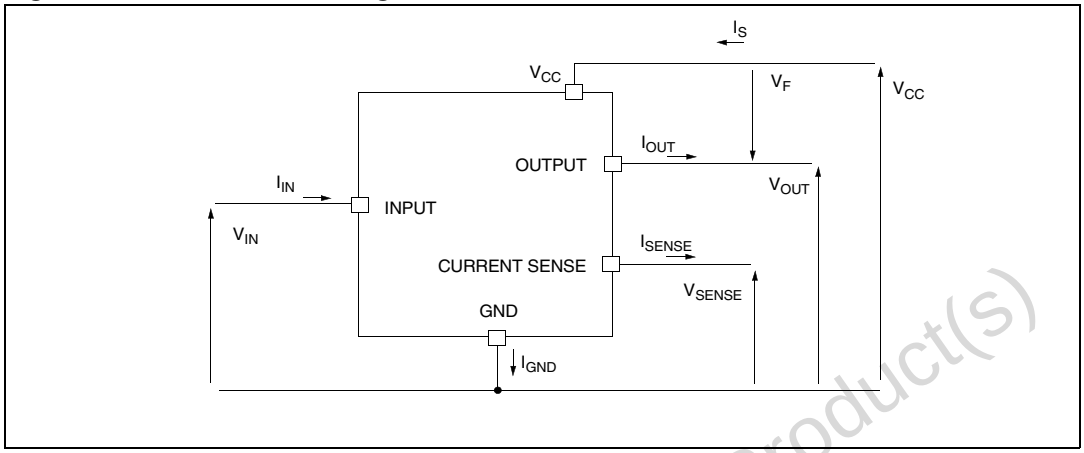
SO-16L

Table 2. Suggested connections for unused and not connected pins

Connection / pin	Current Sense	N.C.	Output	Input
Floating		X	X	X
To ground	Through 1KΩ resistor	X		Through 10KΩ resistor

2 Electrical specifications

Figure 3. Current and voltage conventions



2.1 Absolute maximum ratings

Stressing the device above the rating listed in the “Absolute maximum ratings” table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to Absolute maximum rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics sure program and other relevant quality document.

Table 3. Absolute maximum ratings

Symbol	Parameter	Value			Unit
		SO-16L	PENTAWATT	P²PAK	
V_{CC}	DC supply voltage	41			V
- V_{CC}	Reverse DC supply voltage	- 0.3			V
- I_{gnd}	DC reverse ground pin current	- 200			mA
I_{OUT}	DC output current	Internally limited			A
- I_{OUT}	Reverse DC output current	- 21			A
I_{IN}	DC input current	+/- 10			mA
V_{CSENSE}	Current sense maximum voltage	- 3 + 15			V V
V_{ESD}	Electrostatic discharge (human body model: R = 1.5KΩ; C = 100pF) INPUT CURRENT SENSE OUTPUT V_{CC}	 4000 2000 5000 5000			 V V V V

Table 3. Absolute maximum ratings (continued)

Symbol	Parameter	Value			Unit
		SO-16L	PENTAWATT	P^2PAK	
E_{MAX}	Maximum switching energy (L = 0.25mH; R_L= 0Ω; V_{bat} = 13.5V; T_{jstart} = 150ºC; I_L = 45A)	352		364	mJ
P_{tot}	Power dissipation T_C ≤25°C	8.3	96.1	96.1	W
T_j	Junction operating temperature	Internally limited			°C
T_c	Case operating temperature	- 40 to 150			°C
T_{stg}	Storage temperature	- 55 to 150			°C

2.2 Thermal data

Table 4. Thermal data

Symbol	Parameter	Max. value			Unit
		SO-16L	PENTAWATT	P^2PAK	
$R_{thj\text{-}case}$	Thermalresistance junction-case	-	1.3	1.3	°C/W
$R_{thj\text{-}lead}$	Thermalresistance junction-lead	15	-		°C/W
$R_{thj\text{-}amb}$	Thermalresistance junction-ambient	65(1)	61.3	51.3(2)	°C/W
		48(3)		37(4)	°C/W

1. When mounted on a standard single-sided FR-4 board with 0.5cm2 of Cu (at least 35µm thick) connected to all VCC pins.
2. When mounted on a standard single-sided FR-4 board with 0.5cm2 of Cu (at least 35µm thick).
3. When mounted on a standard single-sided FR-4 board with 6cm2 of Cu (at least 35µm thick) connected to all VCC pins.
4. When mounted on a standard single-sided FR-4 board with 6cm2 of Cu (at least 35µm thick).

2.3 Electrical characteristics

Values specified in this section are for 8V < V_{CC} < 36V; -40°C < T_j < 150°C, unless otherwise stated.

Table 5. Power

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{CC}	Operating supply voltage		5.5	13	36	V
V_{USD}	Under-voltage shutdown		3	4	5.5	V
V_{OV}	Over-voltage shutdown		36			V
R_{ON}	On-state resistance	I_{OUT} = 10A; T_j = 25°C; I_{OUT} = 10A; I_{OUT} = 3A; V_{CC} = 6V			16 32 55	mΩ mΩ mΩ
V_{CLAMP}	Clamp voltage	I_{CC} = 20mA	41	48	55	V
I_S	Supply current	Off-state; V_{CC} = 13V; V_{IN} = V_{OUT} = 0V Off-state; V_{CC} = 13V; V_{IN} = V_{OUT} = 0V; T_j = 25°C On-state; V_{CC} = 13V; V_{IN} = 5V; I_{OUT} = 0A; R_{SENSE} = 3.9 kΩ		10 10	25 20 5	µA µA mA
$I_{L(off1)}$	Off-state output current	V_{IN} = V_{OUT} = 0V	0		50	µA
$I_{L(off2)}$	Off-state output current	V_{IN} = 0V; V_{OUT} = 3.5V	-75		0	µA
$I_{L(off3)}$	Off-state output current	V_{IN} = V_{OUT} = 0V; V_{CC} = 13V; T_j = 125°C			5	µA
$I_{L(off4)}$	Off-state output current	V_{IN} = V_{OUT} = 0V; V_{CC} = 13V; T_j = 25°C			3	µA

Note: V_{CLAMP} and V_{OV} are correlated. Typical difference is 5V.

Table 6. Switching (V_{CC}=13V)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	R_L = 1.3Ω (see *Figure 4.*)		50		µs
$t_{d(off)}$	Turn-off delay time	R_L = 1.3Ω (see *Figure 4.*)		50		µs
$dV_{OUT}/dt_{(on)}$	Turn-on voltage slope	R_L = 1.3Ω (see *Figure 4.*)	See *Figure 10.*			V/µs
$dV_{OUT}/dt_{(off)}$	Turn-off voltage slope	R_L = 1.3Ω (see *Figure 4.*)	See *Figure 12.*			V/µs

Table 7. Logic inputs

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{IL}	Input low level voltage				1.25	V
I_{IL}	Low level input current	V_{IN} = 1.25V	1			µA
V_{IH}	Input high-level voltage		3.25			V
I_{IH}	High-level input current	V_{IN} = 3.25V			10	µA
$V_{I(hyst)}$	Input hysteresis voltage		0.5			V
V_{ICL}	Input clamp voltage	I_{IN} = 1mA I_{IN} = - 1mA	6	6.8 - 0.7	8	V V

Table 8. Current sense (9V ≤V_{CC} ≤16V)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
K_1	I_{OUT}/I_{SENSE}	I_{OUT} = 1A; V_{SENSE} = 0.5V; T_j = -40°C...150°C	3300	4400	6000	
dK_1/K_1	Current sense ratio drift	I_{OUT} = 1A; V_{SENSE} = 0.5V; T_j= - 40°C...150°C	-10		+10	%
K_2	I_{OUT}/I_{SENSE}	I_{OUT} = 10A; V_{SENSE} = 4V; T_j = - 40°C T_j= 25°C...150°C	4200 4400	4900 4900	6000 5750	
dK_2/K_2	Current sense ratio drift	I_{OUT} = 10A; V_{SENSE} = 4V; T_j = -40°C...150°C	-8		+8	%
K_3	I_{OUT}/I_{SENSE}	I_{OUT} = 30A; V_{SENSE} = 4V; T_j = -40°C T_j = 25°C...150°C	4200 4400	4900 4900	5500 5250	
dK_3/K_3	Current sense ratio drift	I_{OUT} = 30A; V_{SENSE} = 4V; T_j = -40°C...150°C	-6		+6	%
I_{SENSE0}	Analog sense current	V_{CC} = 6...16V; I_{OUT} = 0A; V_{SENSE} = 0V; T_j = -40°C...150°C	0		10	µA
V_{SENSE}	Max analog sense output voltage	V_{CC} = 5.5V; I_{OUT} = 5A; R_{SENSE} = 10kΩ V_{CC} > 8V, I_{OUT} = 10A; R_{SENSE} = 10kΩ	2 4			V V
V_{SENSEH}	Sense voltage in over-temperature condition	V_{CC} = 13V; R_{SENSE} = 3.9kΩ		5.5		V

Table 8. Current sense (9V ≤V_{CC} ≤16V) (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$R_{VSENSEH}$	Analog sense output impedance in over-temperature condition	V_{CC} = 13V; T_j > T_{TSD}; output open		400		Ω
t_{DSENSE}	Current sense delay response	To 90% I_{SENSE} (1)			500	µs

1. Current sense signal delay after positive input slope.

Table 9. V_{CC} output diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_F	Forward on voltage	- I_{OUT} = 5A; T_j = 150°C			0.6	V

Table 10. Protections(1)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
T_{TSD}	Shutdown temperature		150	175	200	°C
T_R	Reset temperature		135			°C
T_{hyst}	Thermal hysteresis		7	15		°C
I_{lim}	Current limitation	V_{CC} = 13V 5V < V_{CC} < 36V	30	45	75 75	A A
V_{demag}	Turn-off output clamp voltage	I_{OUT} = 2 A; V_{IN} = 0V; L = 6mH	V_{CC} - 41	V_{CC} - 48	V_{CC} - 55	V
V_{ON}	Output voltage drop limitation	I_{OUT} = 1 A; T_j = -40°C...150°C		50		mV

1. To ensure long term reliability under heavy over-load or short circuit conditions, protection and related diagnostic signals must be used together with a proper software strategy. If the device operates under abnormal conditions this software must limit the duration and number of activation cycles.

Table 11. Truth table

Conditions	Input	Output	Sense
Normal operation	L H	L H	0 Nominal
Over-temperature	L H	L L	0 V_{SENSEH}
Under-voltage	L H	L L	0 0
Over-voltage	L H	L L	0 0
Short circuit to GND	L H H	L L L	0 (T_j<T_{TSD}) 0 (T_j>T_{TSD}) V_{SENSEH}
Short circuit to V_{CC}	L H	H H	0 < Nominal
Negative output voltage clamp	L	L	0

Table 12. Electrical transient requirements

ISO T/R 7637/1 Test pulse	Test level				
	I	II	III	IV	Delays and impedance
1	- 25V(1)	- 50V(1)	- 75V(1)	- 100V(1)	2ms, 10Ω
2	+ 25V(1)	+ 50V(1)	+ 75V(1)	+ 100V(1)	0.2ms, 10Ω
3a	- 25V(1)	- 50V(1)	- 100V(1)	- 150V(1)	0.1µs, 50Ω
3b	+ 25V(1)	+ 50V(1)	+ 75V(1)	+ 100V(1)	0.1µs, 50Ω
4	- 4V(1)	- 5V(1)	- 6V(1)	- 7V(1)	100ms, 0.01Ω
5	+ 26.5V(1)	+ 46.5V(2)	+ 66.5V(2)	+ 86.5V(2)	400ms, 2Ω

1. All functions of the device are performed as designed after exposure to disturbance.
2. One or more functions of the device is not performed as designed after exposure and cannot be returned to proper operation without replacing the device.

Figure 4. Switching characteristics

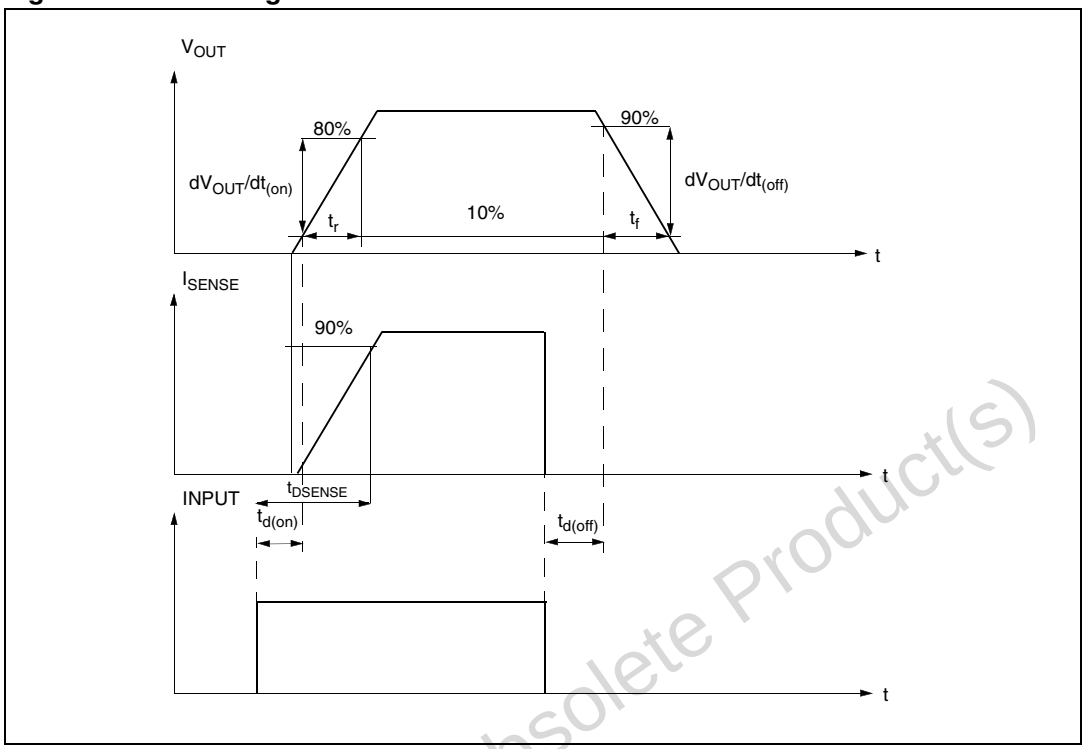


Figure 5. I_{OUT}/I_{SENSE} versus I_{OUT}

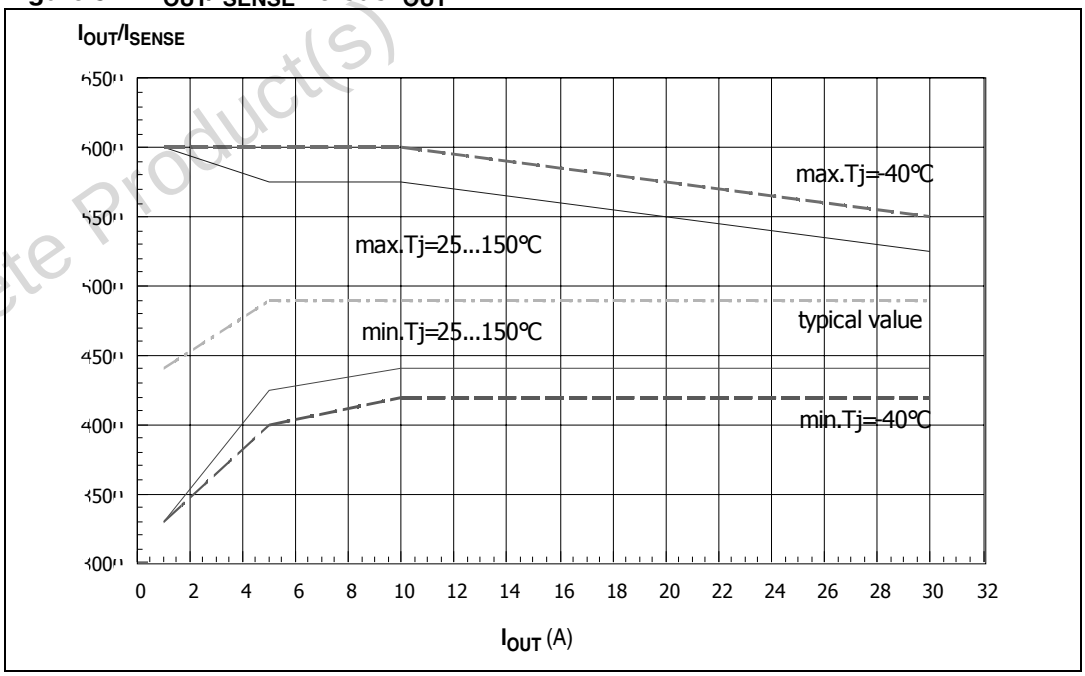
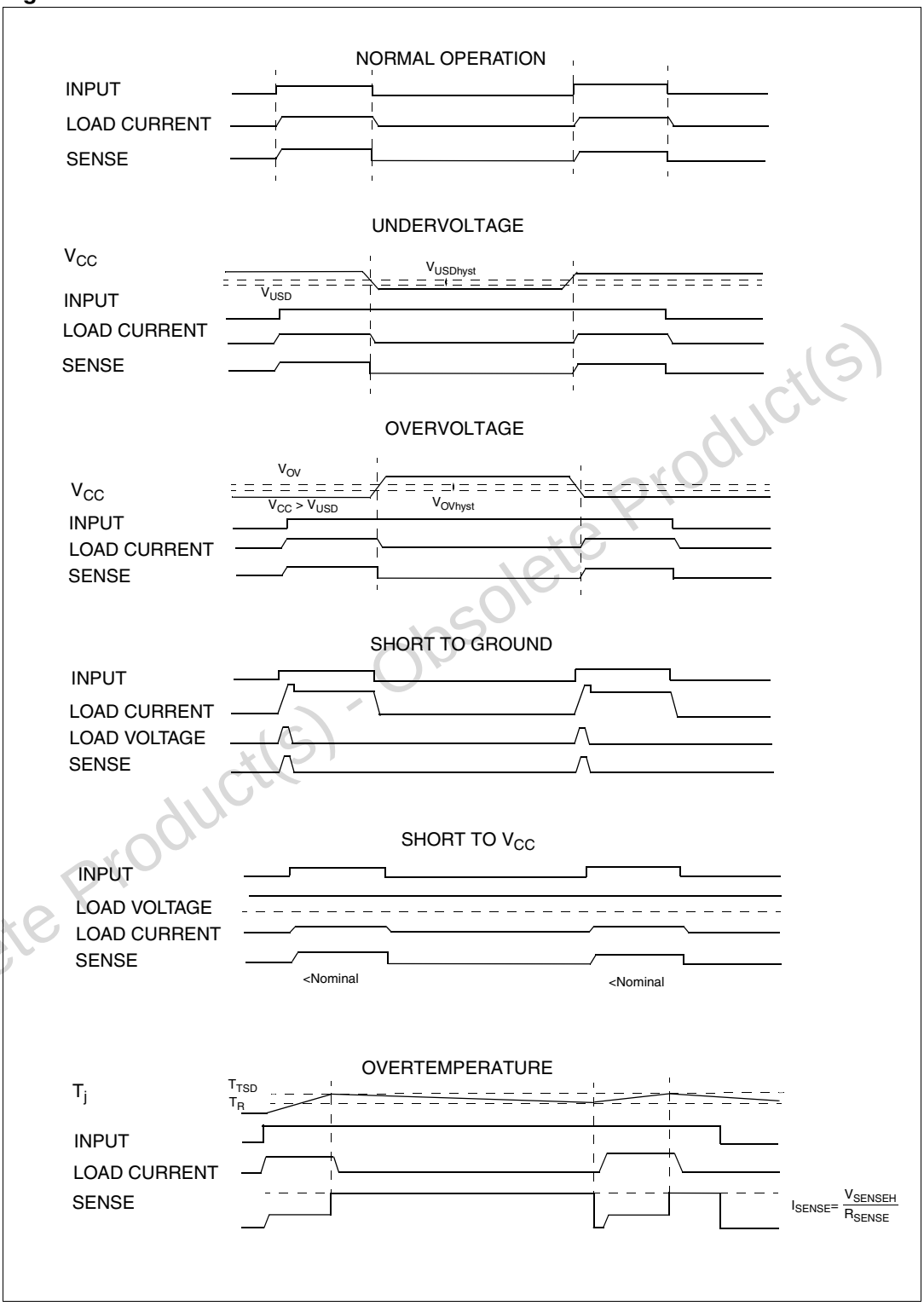


Figure 6. Waveforms



2.4 Electrical characteristics curves

Figure 7. Off-state output current

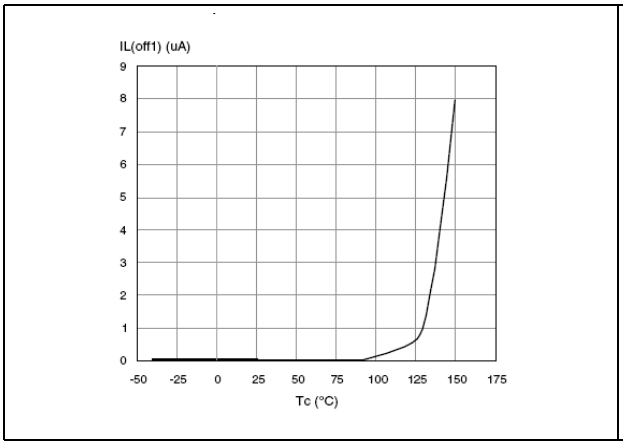


Figure 8. High-level input current

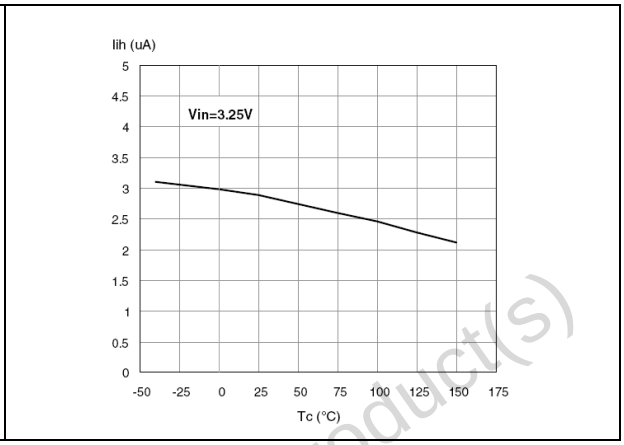


Figure 9. Input clamp voltage

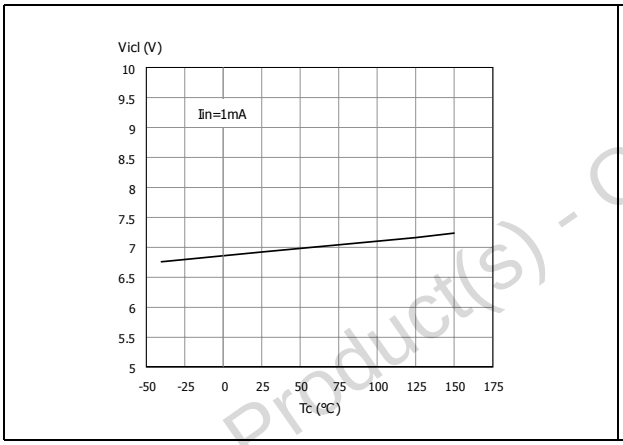


Figure 10. Turn-on voltage slope

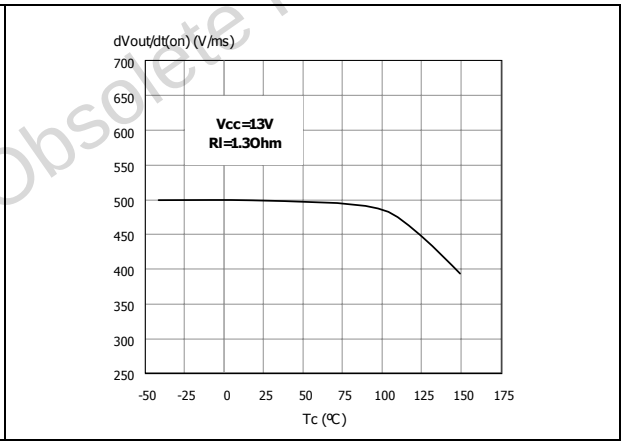


Figure 11. Over-voltage shutdown

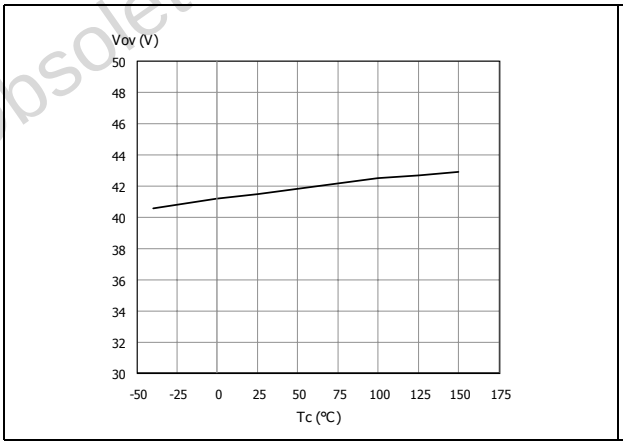


Figure 12. Turn-off voltage slope

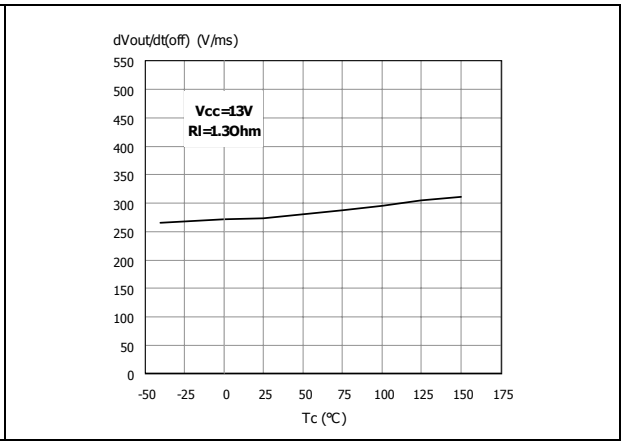


Figure 13. I_{LIM} vs T_{case}

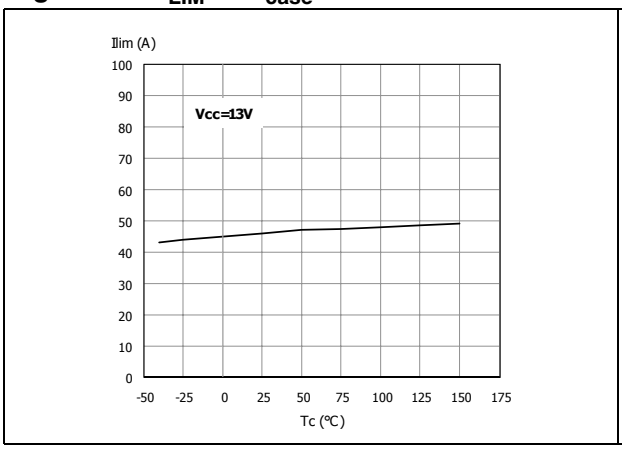


Figure 14. On-state resistance vs V_{CC}

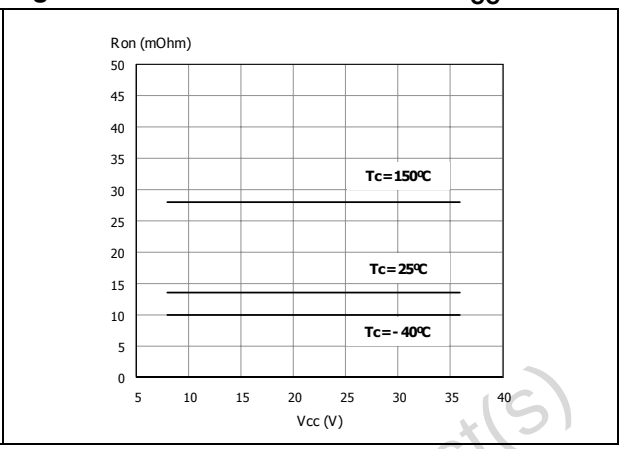


Figure 15. Input high-level

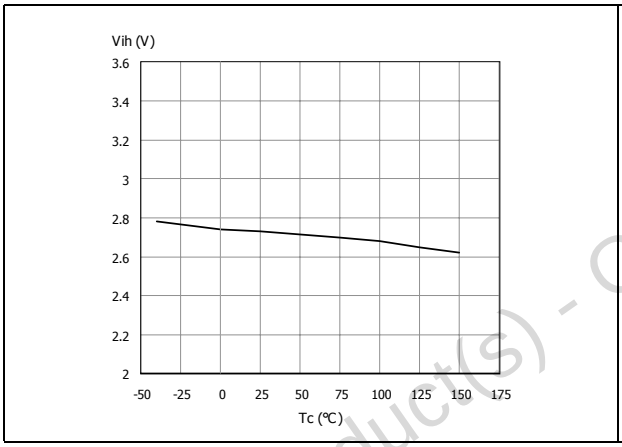


Figure 16. Input hysteresis voltage

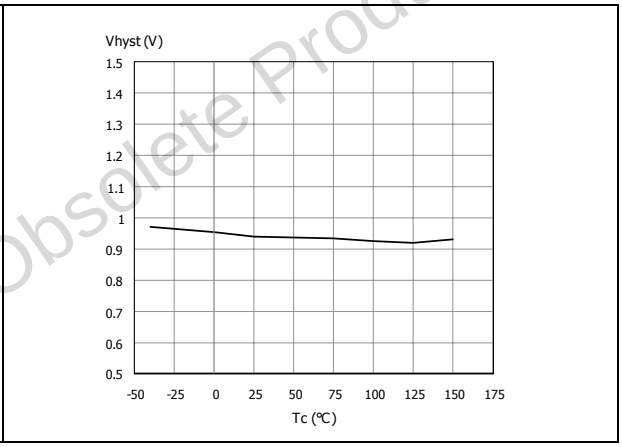


Figure 17. On-state resistance vs Tcase

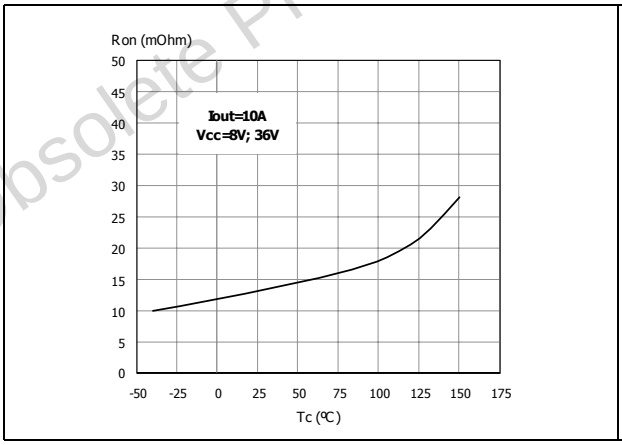
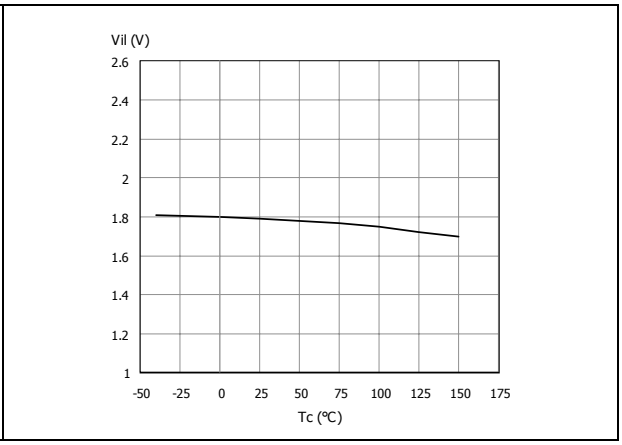
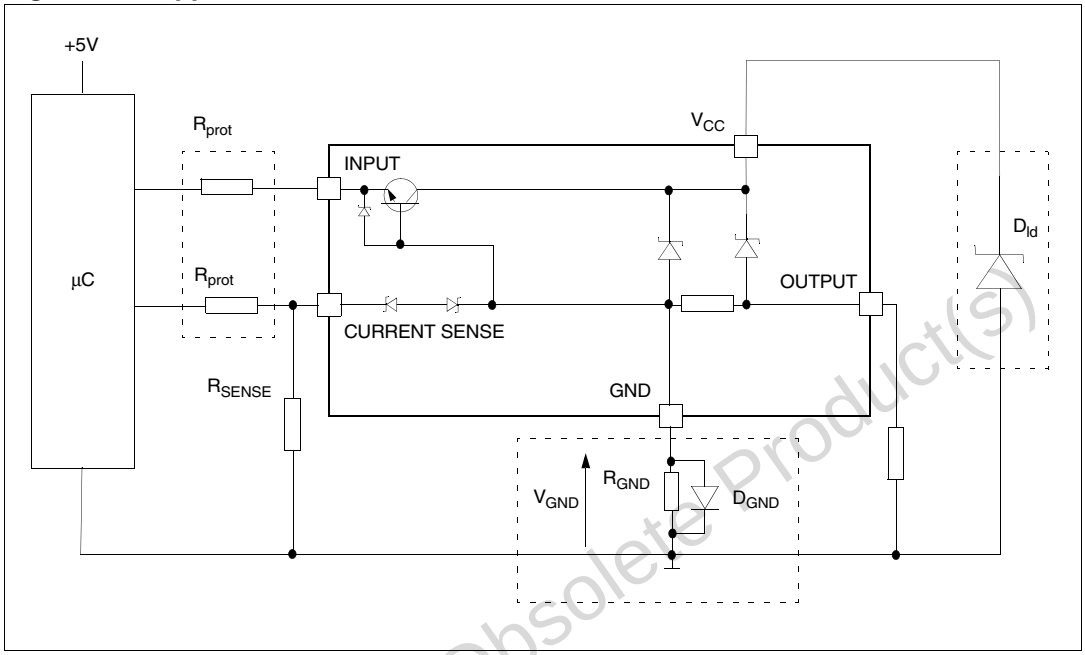


Figure 18. Input low level



3 Application information

Figure 19. Application schematic



3.1 GND protection network against reverse battery

3.1.1 Solution 1: resistor in the ground line (R_{GND} only)

This can be used with any type of load.

The following is an indication on how to dimension the R_{GND} resistor.

1. $R_{GND} \leq 600mV / (I_{S(on)max})$.
2. $R_{GND} \geq (- V_{CC}) / (- I_{GND})$

where $- I_{GND}$ is the DC reverse ground pin current and can be found in the absolute maximum rating section of the device datasheet.

Power Dissipation in R_{GND} (when $V_{CC} < 0$: during reverse battery situations) is:

$P_D = (- V_{CC})^2 / R_{GND}$

This resistor can be shared amongst several different HSDs. Please note that the value of this resistor should be calculated with formula (1) where $I_{S(on)max}$ becomes the sum of the maximum on-state currents of the different devices.

Please note that if the microprocessor ground is not shared by the device ground then the R_{GND} will produce a shift ($I_{S(on)max} * R_{GND}$) in the input thresholds and the status output values. This shift will vary depending on how many devices are ON in the case of several high-side drivers sharing the same R_{GND}.

If the calculated power dissipation leads to a large resistor or several devices have to share the same resistor then ST suggests to utilize Solution 2 (see below).

3.1.2 Solution 2: diode (D_{GND}) in the ground line

A resistor (R_{GND} = 1kΩ) should be inserted in parallel to D_{GND} if the device drives an inductive load.

This small signal diode can be safely shared amongst several different HSDs. Also in this case, the presence of the ground network will produce a shift (≈ 600mV) in the input threshold and in the status output values if the microprocessor ground is not common to the device ground. This shift will not vary if more than one HSD shares the same diode/resistor network.

Series resistor in INPUT and STATUS lines are also required to prevent that, during battery voltage transient, the current exceeds the absolute maximum rating.

Safest configuration for unused INPUT and STATUS pin is to leave them unconnected.

3.2 Load dump protection

D_{ld} is necessary (Voltage Transient Suppressor) if the load dump peak voltage exceeds the V_{CC} max DC rating. The same applies if the device is subject to transients on the V_{CC} line that are greater than the ones shown in the ISO 7637-2: 2004(E) table.

3.3 MCU I/Os protection

If a ground protection network is used and negative transient are present on the V_{CC} line, the control pins will be pulled negative. ST suggests to insert a resistor (R_{prot}) in line to prevent the µC I/Os pins to latch-up.

The value of these resistors is a compromise between the leakage current of µC and the current required by the HSD I/Os (Input levels compatibility) with the latch-up limit of µC I/Os.

$-V_{CCpeak}/I_{latchup} \leq R_{prot} \leq (V_{OH\mu C}-V_{IH}-V_{GND}) / I_{IHmax}$

Calculation example:

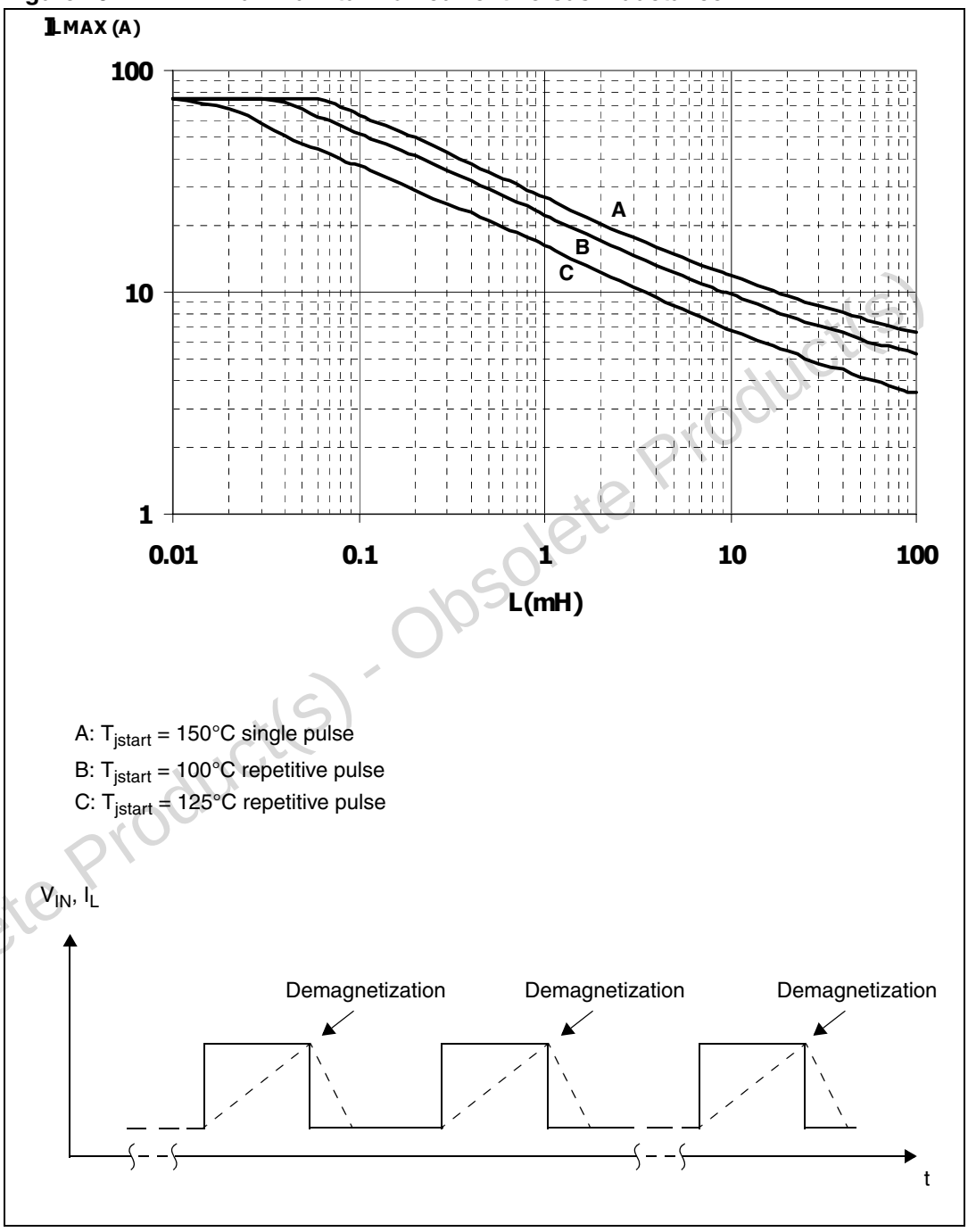
For V_{CCpeak}= - 100V and $I_{latchup} \geq$ 20mA; $V_{OH\mu C} \geq$ 4.5V

5kΩ $\leq R_{prot} \leq$ 65kΩ

Recommended values: R_{prot} =10kΩ.

3.4 P²PAK maximum demagnetization energy (V_{CC} = 13.5V)

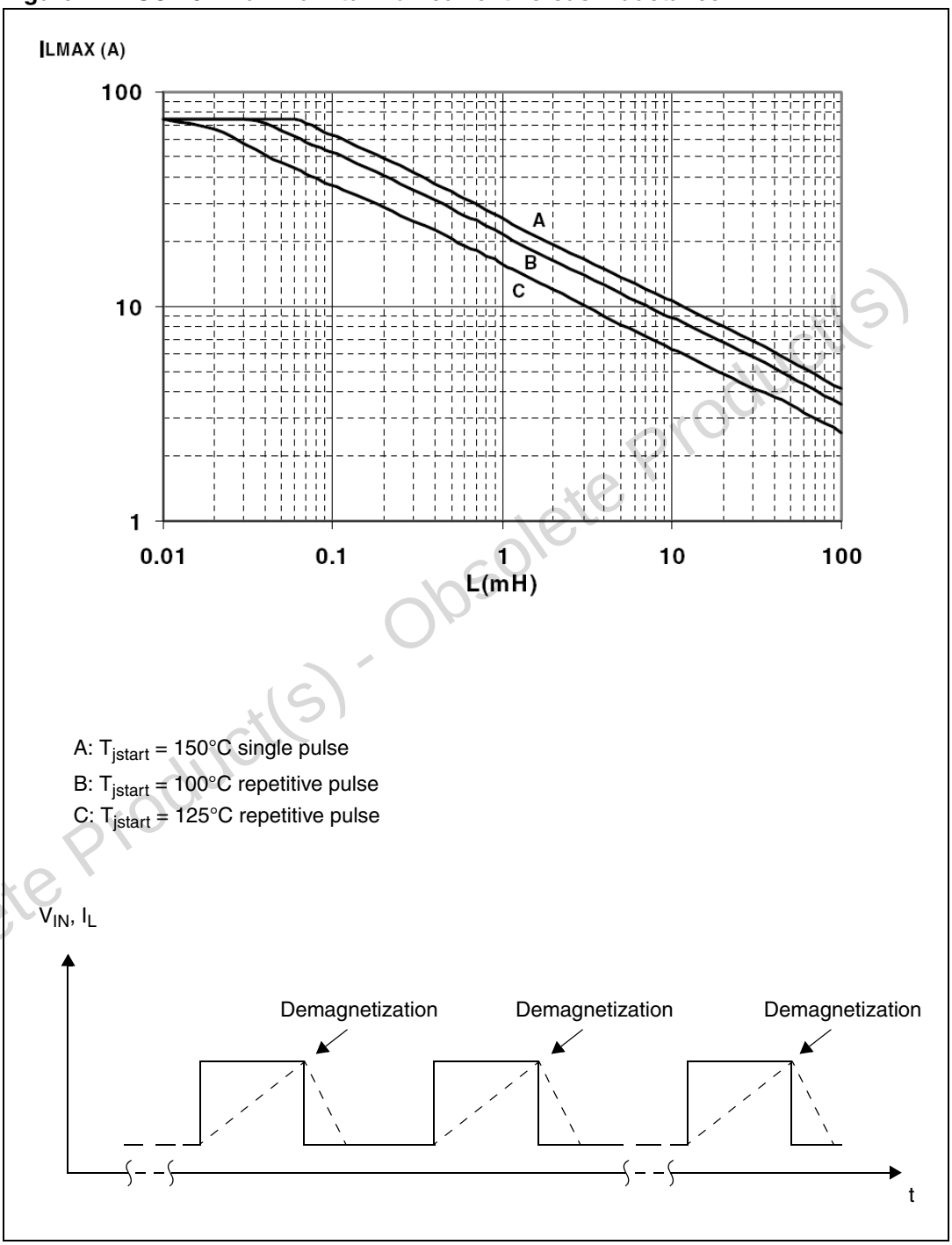
Figure 20. P²PAK maximum turn-off current versus inductance



Note: Values are generated with R_L =0 Ω In case of repetitive pulses, T_{jstart} (at beginning of each demagnetization) of every pulse must not exceed the temperature specified above for curves A and B.

3.5 SO-16L maximum demagnetization energy (V_{CC} = 13.5V)

Figure 21. SO-16L maximum turn-off current versus inductance

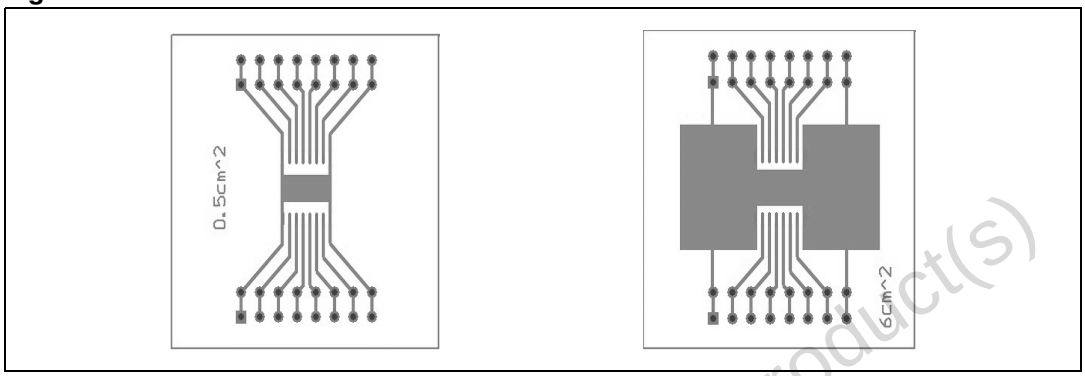


Note: Values are generated with R_L =0 Ω In case of repetitive pulses, T_{jstart} (at beginning of each demagnetization) of every pulse must not exceed the temperature specified above for curves A and B.

4 Package and PCB thermal data

4.1 SO-16L thermal data

Figure 22. SO-16L PC board



Note: Layout condition of R_{th} and Z_{th} measurements (PCB FR4 area = 41mm x 48mm, PCB thickness = 2mm, Cu thickness = 35µm, Copper areas: 0.5cm^2, 6cm^2).

Figure 23. SO-16L $R_{thj\text{-}amb}$ Vs PCB copper area in open box free air condition

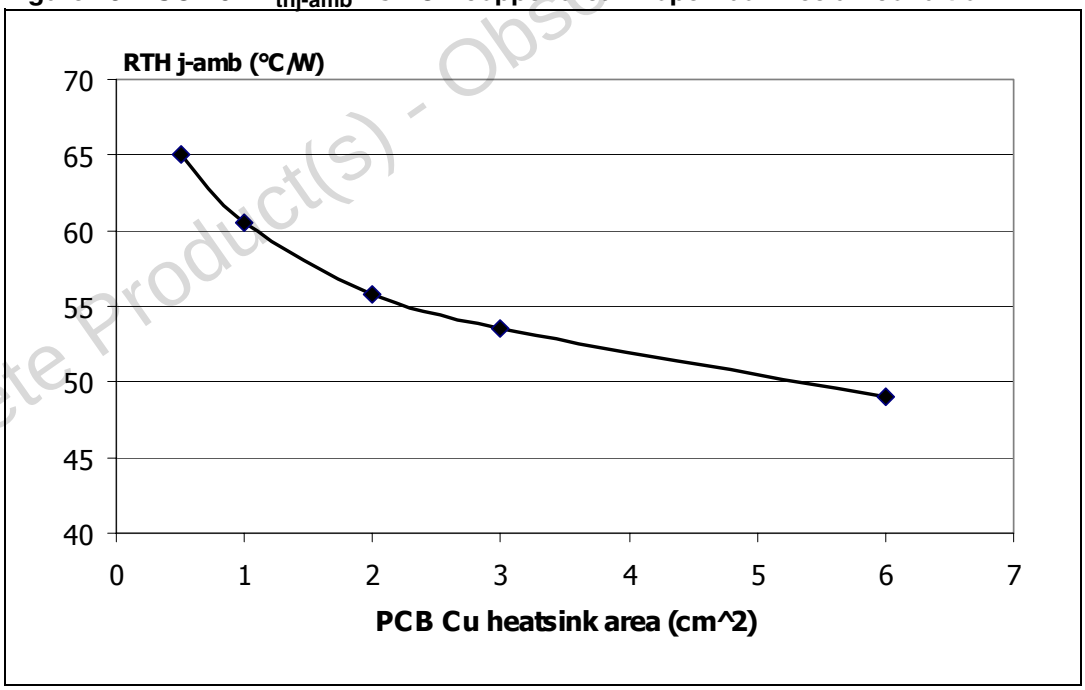
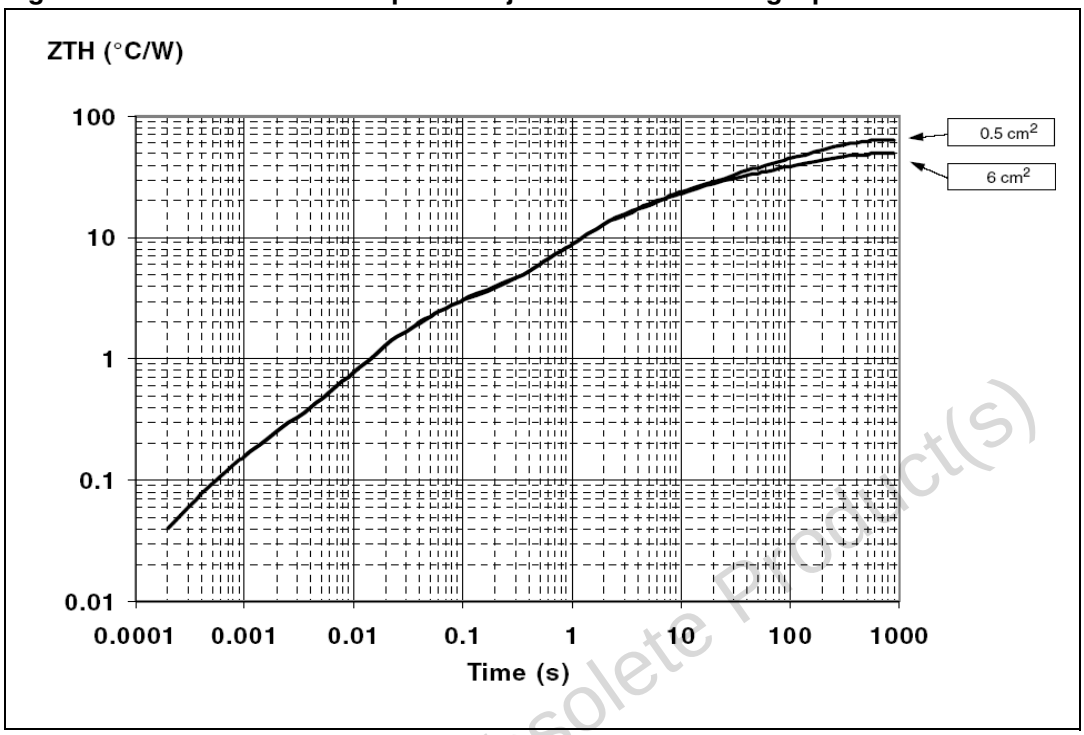


Figure 24. SO-16L thermal impedance junction ambient single pulse



Equation 1: pulse calculation formula

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1 - \delta)$$

where $\delta = t_p / T$

Figure 25. Thermal fitting model of a single channel HSD in SO-16L

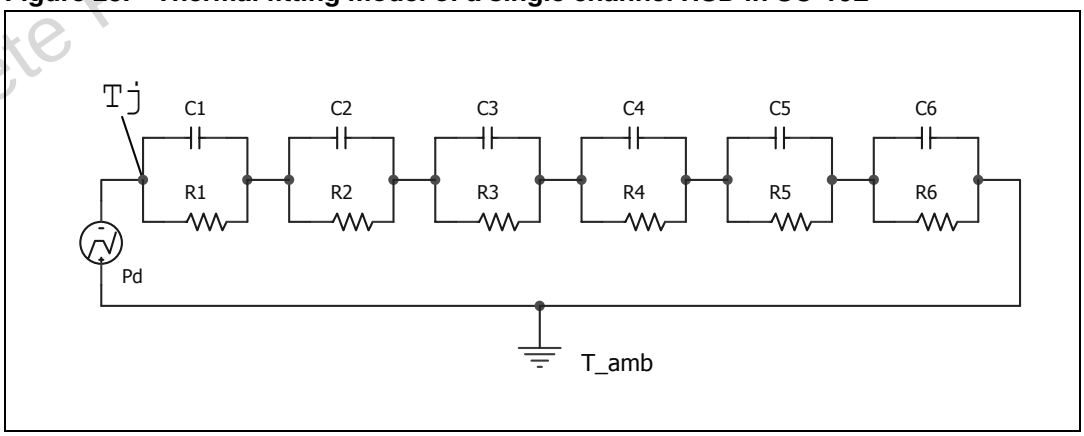
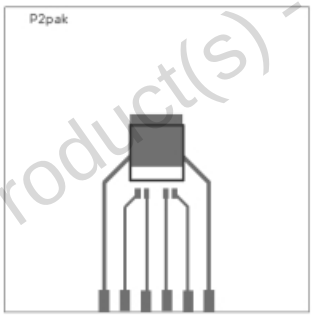


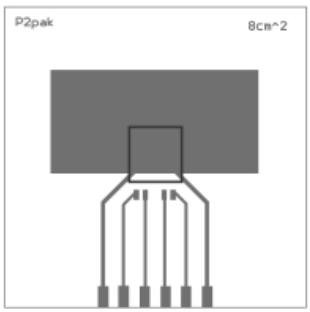
Table 13. SO-16L thermal parameters

Area / island (cm^2)	Footprint	6
R1 (°C/W)	0.02	
R2 (°C/W)	0.1	
R3 (°C/W)	2.2	
R4 (°C/W)	12	
R5 (°C/W)	15	
R6 (°C/W)	35	20
C1 (W.s/°C)	0.0015	
C2 (W.s/°C)	7E-03	
C3 (W.s/°C)	1.5E-02	
C4 (W.s/°C)	0.14	
C5 (W.s/°C)	1	
C6 (W.s/°C)	5	8

4.2 P^2PAK thermal data

Figure 26. P^2PAK PC board





Note: Layout condition of R_{th} and Z_{th} measurements (PCB FR4 area = 60mm x 60mm, PCB thickness = 2 mm, Cu thickness = 35µm , Copper areas: 0.97cm^2, 8cm^2).

Figure 27. P^2PAK $R_{thj-amb}$ Vs. PCB copper area in open box free air condition

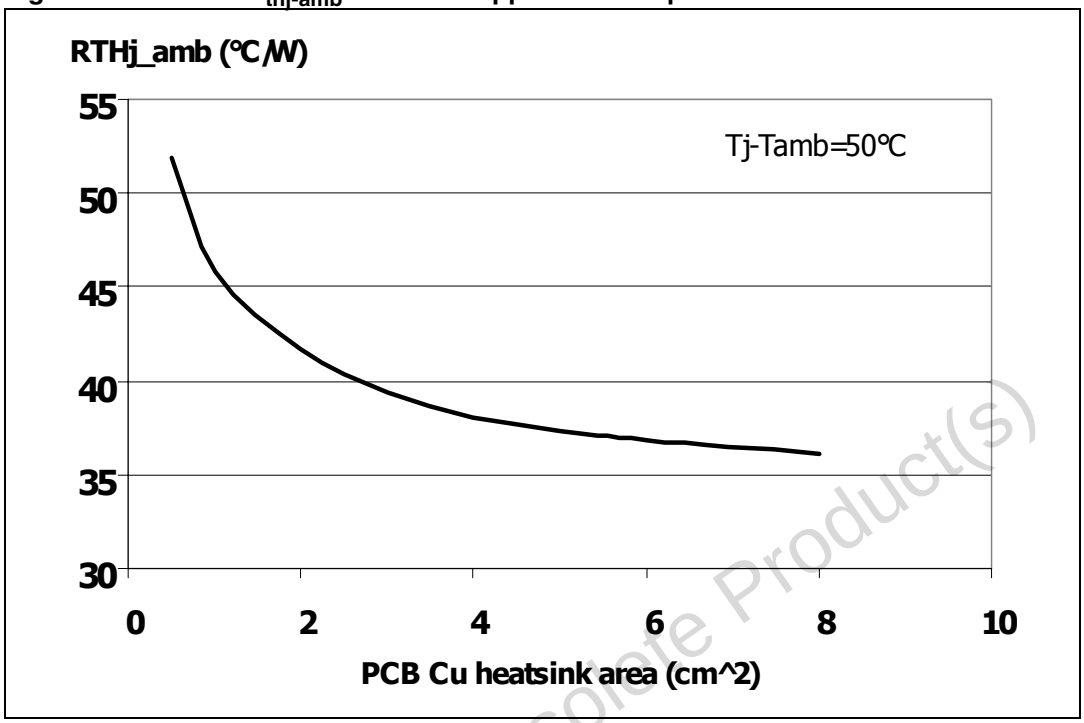
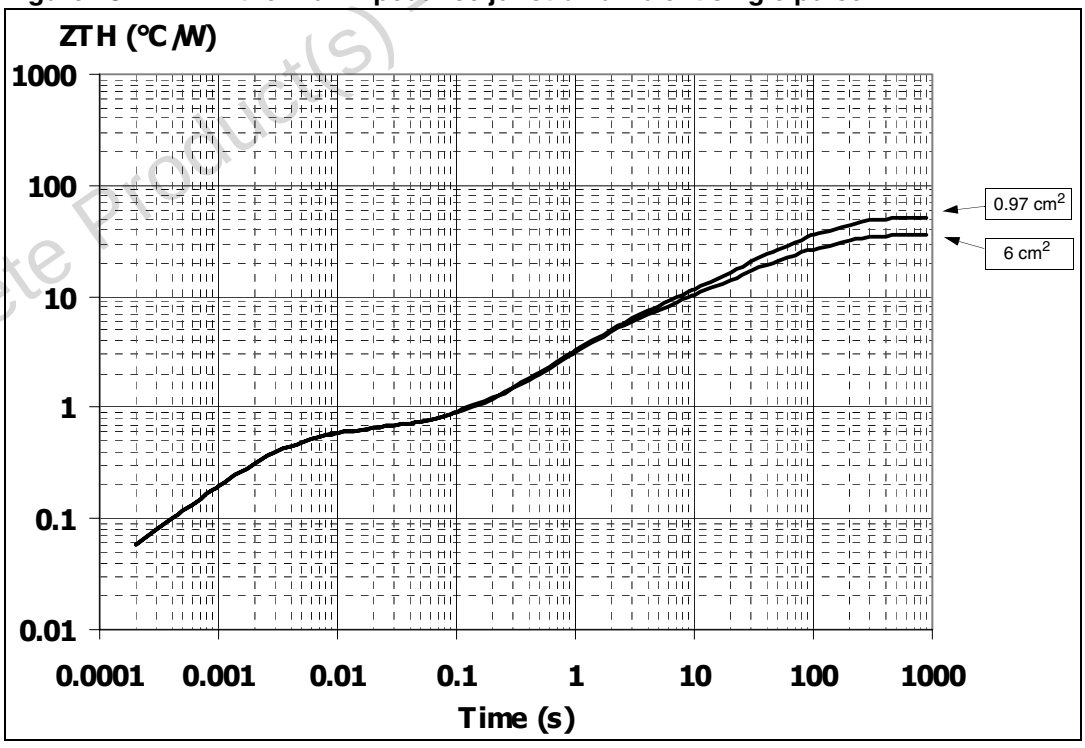


Figure 28. P^2PAK thermal impedance junction ambient single pulse



Equation 2: pulse calculation formula

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1 - \delta)$$

where $\delta = t_P/T$

Figure 29. Thermal fitting model of a single channel HSD in P²PAK

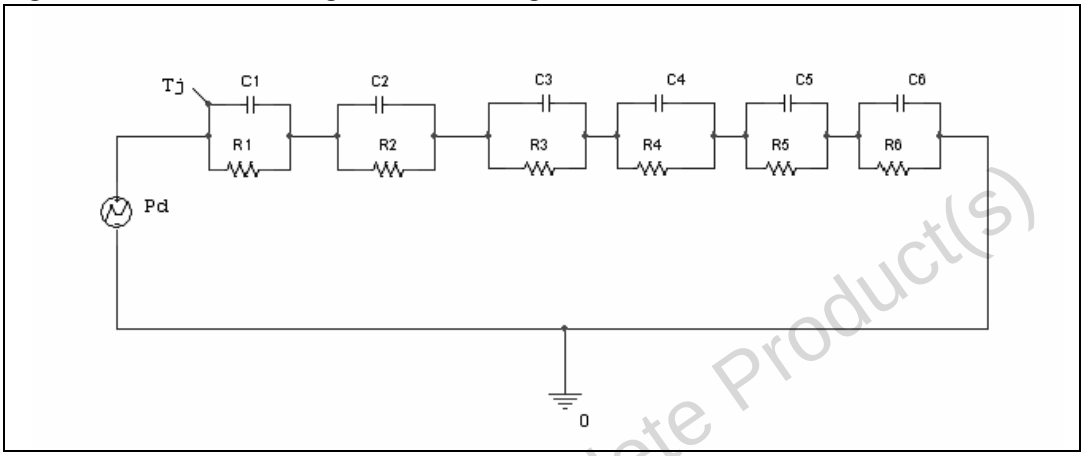


Table 14. P²PAK thermal parameter

Area/island (cm²)	0.97	6
R1 (°C/W)	0.02	
R2 (°C/W)	0.1	
R3 (°C/W)	0.22	
R4 (°C/W)	4	
R5 (°C/W)	9	
R6 (°C/W)	37	22
C1 (W·s/°C)	0.0015	
C2 (W·s/°C)	0.007	
C3 (W·s/°C)	0.015	
C4 (W·s/°C)	0.4	
C5 (W·s/°C)	2	
C6 (W·s/°C)	3	5

5 Package and packing information

5.1 ECOPACK® packages

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

Figure 30. SO-16L package dimensions

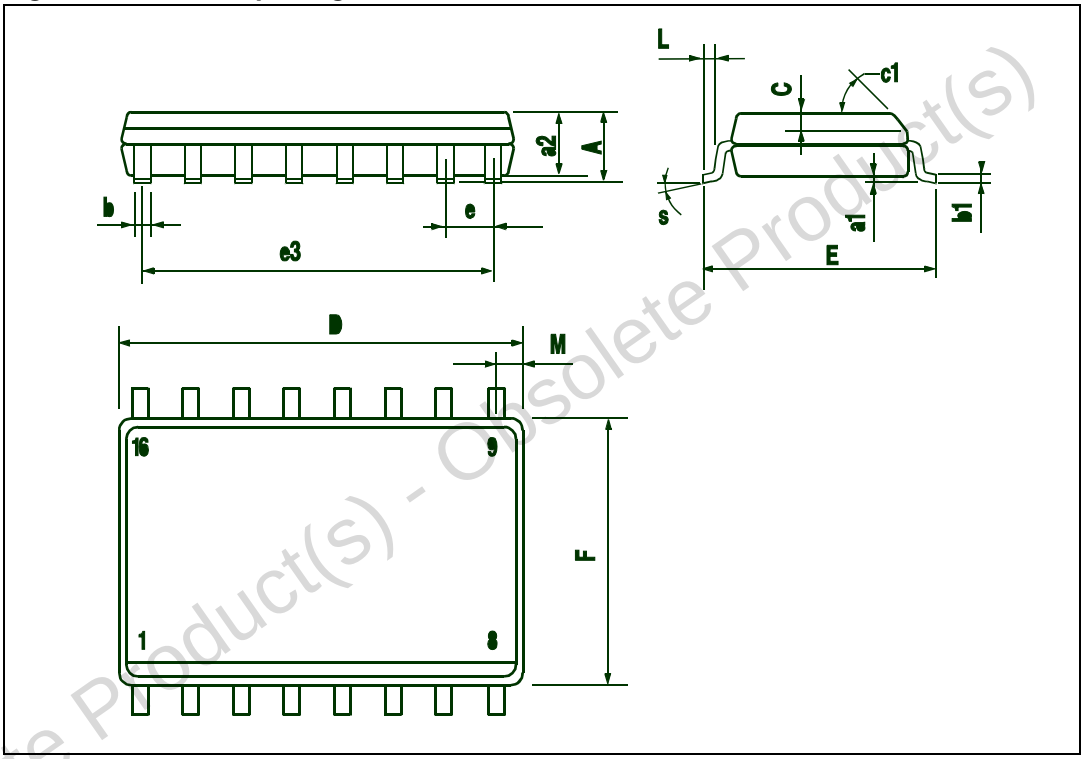


Table 15. SO-16L mechanical data

DIM.	mm.		
	Min.	Typ.	Max.
A			2.65
a1	0.1		0.2
a2			2.45
b	0.35		0.49
b1	0.23		0.32
C		0.5	
c1	45° (typ.)		

Table 15. SO-16L mechanical data (continued)

DIM.	mm.		
	Min.	Typ.	Max.
D	10.1		10.5
E	10.0		10.65
e		1.27	
e3		8.89	
F	7.4		7.6
L	0.5		1.27
M			0.75
S	8° (max.)		

5.2 PENTAWATT mechanical data

Figure 31. PENTAWATT package dimensions

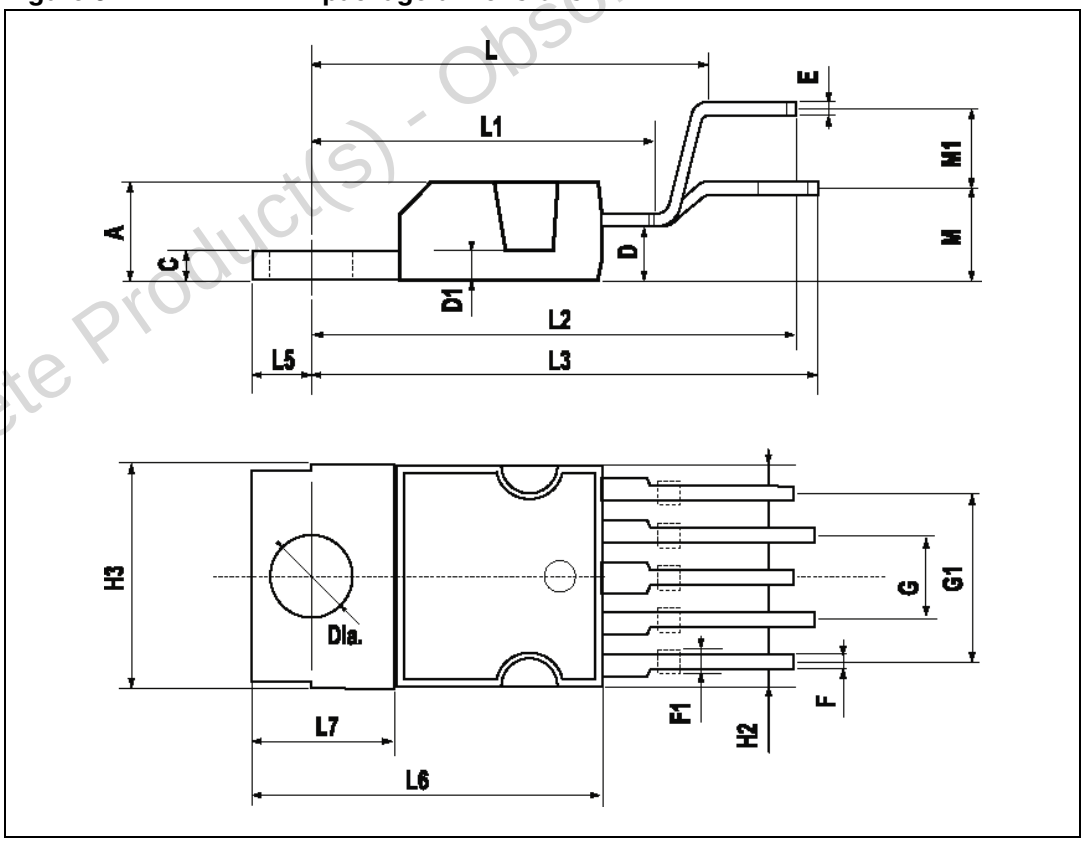


Table 16. PENTAWATT mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A			4.8
C			1.37
D	2.4		2.8
D1	1.2		1.35
E	0.35		0.55
F	0.8		1.05
F1	1		1.4
G	3.2	3.4	3.6
G1	6.6	6.8	7
H2			10.4
H3	10.05		10.4
L		17.85	
L1		15.75	
L2		21.4	
L3		22.5	
L5	2.6		3
L6	15.1		15.8
L7	6		6.6
M		4.5	
M1		4	
Diam.	3.65		3.85

5.3 P²PAK mechanical data

Figure 32. P²PAK package dimensions

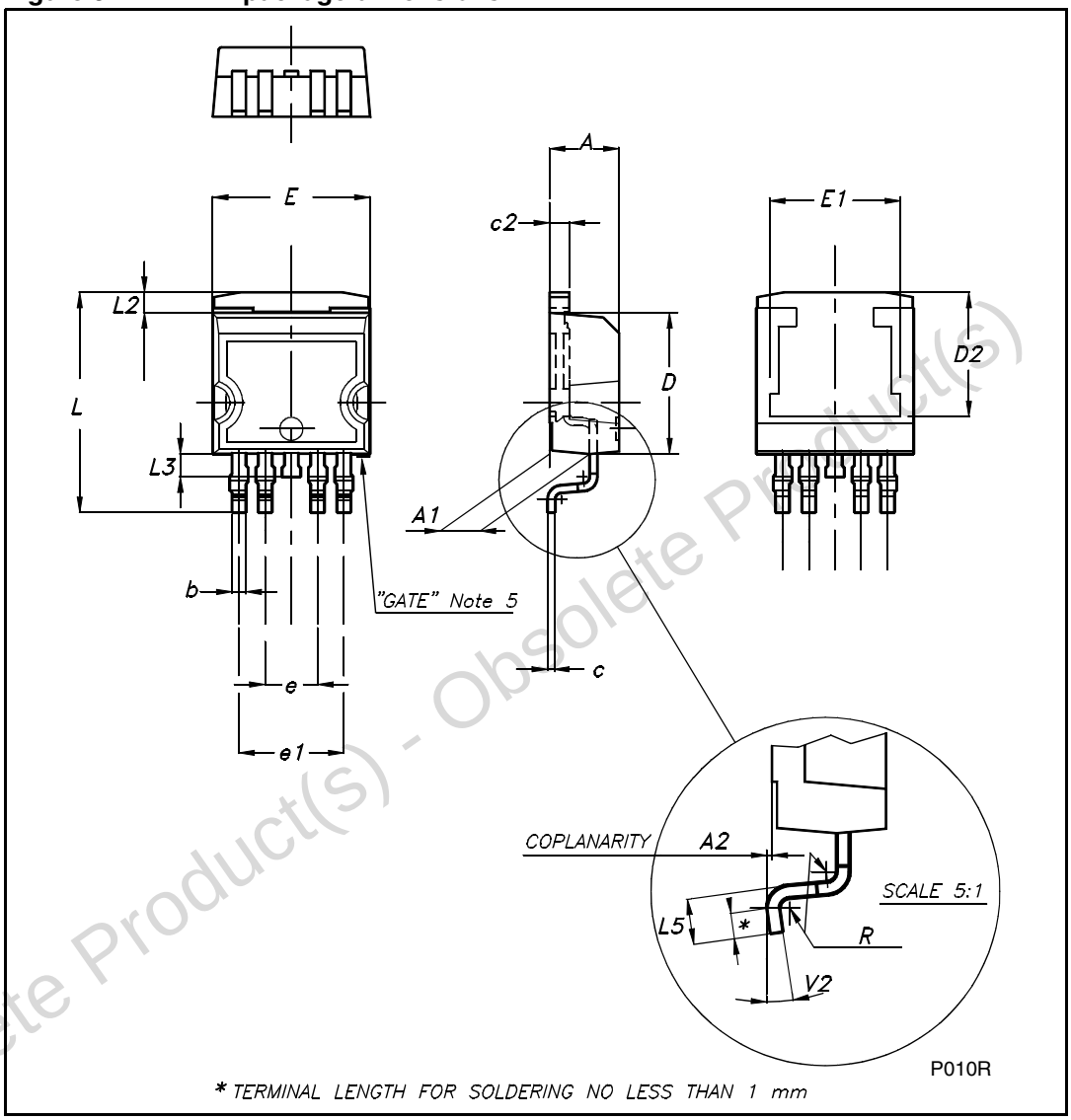
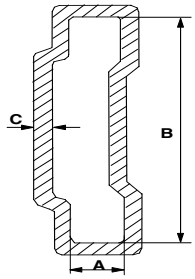


Table 17. P^2PAK mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.30		4.80
A1	2.40		2.80
A2	0.03		0.23
b	0.80		1.05
c	0.45		0.60
c2	1.17		1.37
D	8.95		9.35
D2		8.00	
E	10.00		10.40
E1		8.50	
e	3.20		3.60
e1	6.60		7.00
L	13.70		14.50
L2	1.25		1.40
L3	0.90		1.70
L5	1.55		2.40
R		0.40	
V2	0º		8º
Package weight	1.40 Gr (typ)		

5.4 SO-16L packing information

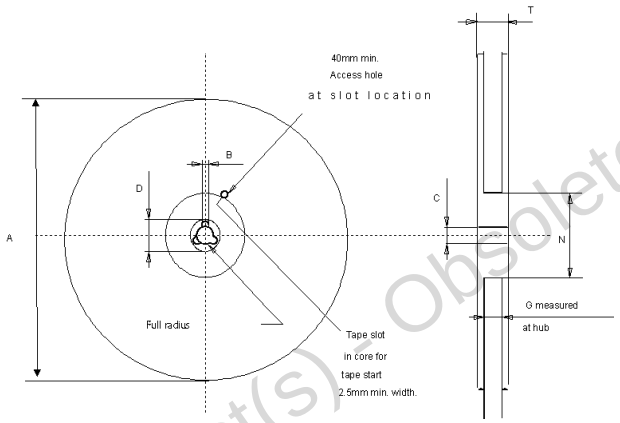
Figure 33. SO-16L tube shipment (no suffix)



Base Q.ty	50
Bulk Q.ty	1000
Tube length (± 0.5)	532
A	3.5
B	13.8
C (± 0.1)	0.6

All dimensions are in mm.

Figure 34. SO-16L tape and reel shipment (suffix "TR")



Reel dimensions

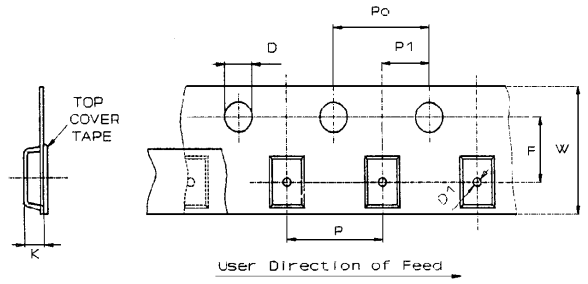
Base Q.ty	1000
Bulk Q.ty	1000
A (max)	330
B (min)	1.5
C (± 0.2)	13
F	20.2
G (+ 2 / -0)	16.4
N (min)	60
T (max)	22.4

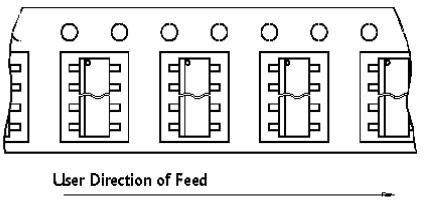
Tape dimensions

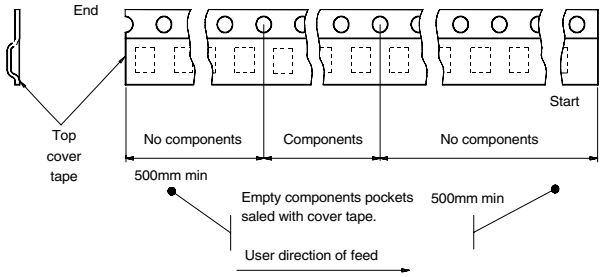
According to Electronic Industries Association (EIA) Standard 481 rev. A, Feb. 1986

Tape width	**W**	16
Tape Hole Spacing	**P0 (± 0.1)**	4
Component Spacing	**P**	12
Hole Diameter	**D (± 0.1/-0)**	1.5
Hole Diameter	**D1 (min)**	1.5
Hole Position	**F (± 0.05)**	7.5
Compartment Depth	**K (max)**	6.5
Hole Spacing	**P1 (± 0.1)**	2

All dimensions are in mm.

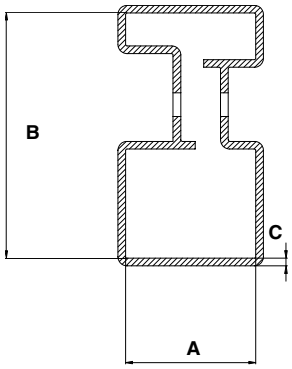






5.5 PENTAWATT packing information

Figure 35. PENTAWATT tube shipment (no suffix)

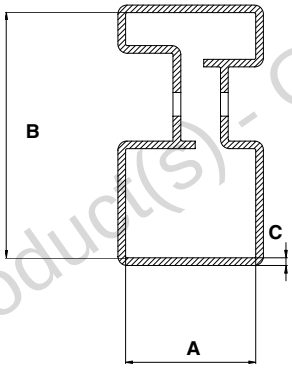


Base Q.ty	50
Bulk Q.ty	1000
Tube length (± 0.5)	532
A	18
B	33.1
C (± 0.1)	1

All dimensions are in mm.

5.6 P^{2}PAK packing information

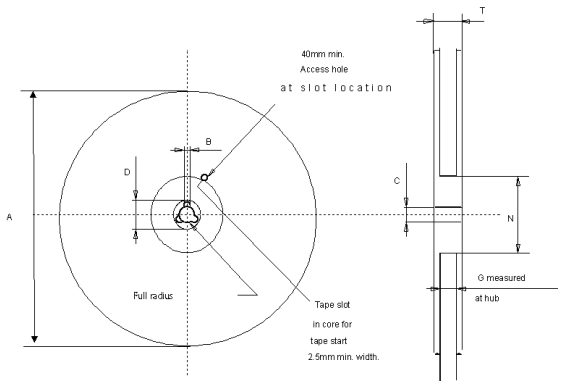
Figure 36. P^{2}PAK tube shipment (no suffix)



Base Q.ty	50
Bulk Q.ty	1000
Tube length (± 0.5)	532
A	18
B	33.1
C (± 0.1)	1

All dimensions are in mm.

Figure 37. P²PAK tape and reel (suffix "13TR")



REEL DIMENSIONS

All dimensions are in mm.

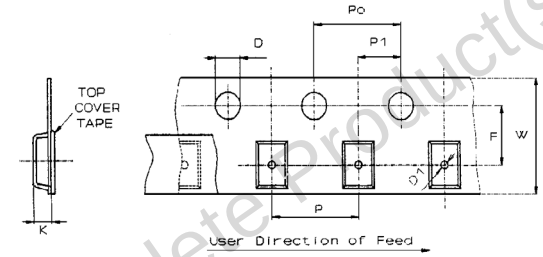
Base Q.ty	1000
Bulk Q.ty	1000
A (max)	330
B (min)	1.5
C (± 0.2)	13
F	20.2
G (+ 2 / -0)	24.4
N (min)	60
T (max)	30.4

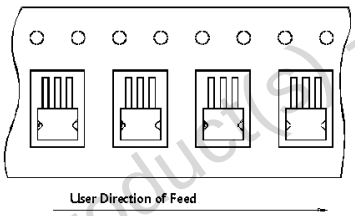
TAPE DIMENSIONS

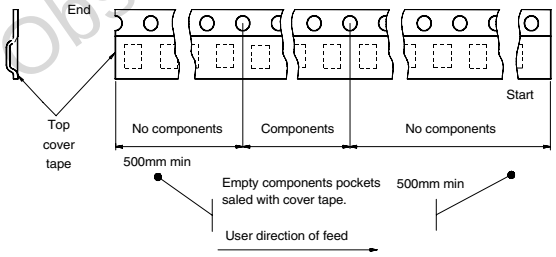
According to Electronic Industries Association (EIA) Standard 481 rev. A, Feb 1986

Tape width	**W**	24
Tape Hole Spacing	**P0 (± 0.1)**	4
Component Spacing	**P**	12
Hole Diameter	**D (± 0.1/-0)**	1.5
Hole Diameter	**D1 (min)**	1.5
Hole Position	**F (± 0.05)**	11.5
Compartment Depth	**K (max)**	6.5
Hole Spacing	**P1 (± 0.1)**	2

All dimensions are in mm.







6 Revision history

Table 18. Document revision history

Date	Revision	Changes
22-Jun-2004	1	Initial release.
07-Jul-2004	2	Current and voltage convention update (page 2). Configuration diagram (top view) & suggested connections for unused and n.c. pins insertion (page 2). 6cm2 Cu condition insertion in thermal data table (page 3).
09-Jul-2004	3	V_{CC} - output diode section update (page 5). Protections note insertion (page 5). Revision history table insertion (page 24). Disclaimers update (page 25).
03-May-2006	4	Suggested connections for unused and n.c.pins? correction (page 2).
17-Dec-2008	5	Document reformatted and restructured. Added content, list of figures and tables. Added *ECOPACK® packages* information. Updated *Figure 37.: P²PAK tape and reel (suffix "13TR")*: changed component spacing (P) in tape dimensions table from 16 mm to 12 mm.
24-Sep-2013	6	Updated Disclaimer.

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